AN IMPROVED SUBTHRESHOLD REGION MODEL FOR SHORT CHANNEL MOSFETS

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by

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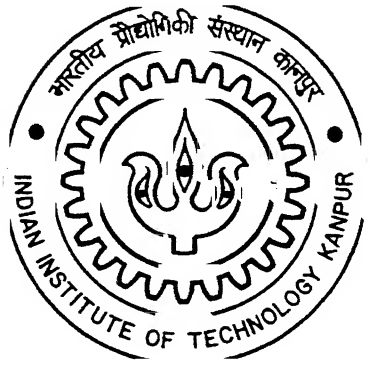

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CERTIFICATE

This is to certify that the work contained in the thesis entitled **"An Improved Subthreshold Region Model for Short Channel MOSFETs"** by **Shivraj B. Thakare** has been carried out under my supervision and that this work has not been submitted elsewhere for the award of a degree.

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Abstract

As analog and mixed-signal VLSI designs are becoming popular, an accurate modeling of the subthreshold region for short channel MOSFETs is becoming extremely important. This region of operation is exploited in modern application areas, such as space electronics, laptops, medical applications, communications, multimedia, etc. Operation of the devices in their subthreshold region reduces the total power dissipation, which is crucial as currently the packing density is increased manyfold due to the rapid advancements in the photolithography techniques. Experimental data on short channel MOSFETs reported in literature show that the subthreshold slope is a function of the applied drain voltage, which previous authors have failed to model. In this work, we have taken up an existing subthreshold slope model (which is independent of the drain voltage) and have modified it to include the effect of the drain voltage. Additionally, our model accounts for the effects of the effective channel length and the body voltage on the subthreshold slope. We have also attempted to represent the fudge factor, used widely in the expression for the characteristic length, by a more physical representation than done before. The subthreshold slope model has been put in an existing drain current model, valid for all regions of operation, in order to obtain the DC characteristics. The simulated results are compared with those reported experimentally for MOSFETs having submicron channel lengths, with the minimum being as small as 0.075 μm. The results show an excellent match between the two.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Invention of the transistor launched a new era of electronic sciences, which created an enormous impact on the modern scientific applications. Very Large Scale Integration (VLSI) is the assembly of millions of such transistors on a single chip known as the Integrated Circuit (IC). These transistors work flawlessly to realize the modern electronics applications in multifarious areas such as multimedia, communication, defense, etc. The advancements in the VLSI technology over the past two decades have significantly influenced every aspect of electronic design, computers and communication systems.

One of the reasons for the popularity of the VLSI systems is the advancements in the fabrication technology which resulted in a very high packing density by reducing the size of the individual transistors on the VLSI chip. The MOS VLSI has always been dominating in the VLSI application area because of continuous reduction in the

size of the MOS transistor. The immediate outcome of the very high packing density is the tremendous increase in the power dissipation in the VLSI chips which needs to be kept within limit. The emergence of products (ICs) having device count in excess of 5 millions using CMOS and BiCMOS technologies and having processing power of the order of 100 millions operations per second or more are challenged by the high-power dissipation. This ultimately led the scientists towards the low power design alternative. Now in the current VLSI scenario, the high speed/low power chips are most viable. The examples of low voltage VLSI systems are wireless communication chips, memory chips and many more battery operated equipment.

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is no longer a device suited only for the digital applications. In the past few years, the semiconductor technology has witnessed the appearance of many MOS chips combining both digital and analog functions. Such ICs are known as the mixed-signal ICs. This trend is likely to continue, since most signal in need of processing are analog at the source, and MOS technology has proved to be suitable for the economical, single chip implementation of analog/digital systems. This trend towards mixed analog/digital chips, not only for the direct interfacing to the physical world, but also for aiding the digital systems to increase their performance will continue in future. The recent examples which are the manifestation of this trend are the disk-drive chip[1] and the analog assisted microprocessor chip[2]. It is predicted that in few years most chips will contain at least some analog circuits in them.

In the era of VLSI, the analog and mixed-signal designs are becoming popular

because of the reasons described above. Also the subthreshold region is getting more importance day by day. Previously, this region was considered mainly for the calculation of the off-stage current in digital ICs because this region was not exploited in the application point of view in digital circuits. Now with the advent of analog ICs, there are quite a few applications where the subthreshold region of operation is exploited, e.g., in digital wrist watches, pacemakers, space electronics, etc.

The computer simulation of the circuits is one of the crucial factors contributing to the success rate of ICs. The circuit simulation is done after the circuit design and prior to the fabrication of the chip. For accurate simulation of the electronic circuits, the device has to be modeled accurately. The device models developed earlier have been proved to be very accurate for long channel MOSFETs. However, for short channel MOSFETs, these models are proved to be quite inaccurate. This is due to the various short channel effects present in miniaturized devices, which are ignored in the long channel MOSFET model development due to their negligible effect on them. However, these effects are the dominant ones for small geometry devices. Hence, the short channel MOSFET modeling in its subthreshold region of operation has become a challenging and important area.

1.1 The Device Modeling

The device model is a mathematical representation of the various physical phenomena occurring in the device. The device model consists of a set of mathematical equations

which are used to predict the behavior of the device accurately under the known excitations of the various input voltages. The device model equations have a set of parameters termed as the model parameters. The model parameters which are used to represent the device phenomenon analytically are referred to as the physical parameters, whereas the ones which are used in the model equations such that these equations are the numerical approximations of the various device phenomena are known as the empirical parameters. The development of the models whose equations are totally based on the analytical representations of the physical phenomena is a difficult task. These models are obviously highly accurate, however, they use up too much of CPU time, and hence, are inefficient for circuit simulation. On the other hand, the totally empirical approach of device model development generating the model having too many empirical parameters is computationally less expensive but also is less accurate and does not always give a true physical picture of the events taking place within the device. Also, the values of these empirical parameters are dependent on the device dimensions and specifications such as effective channel length L_{eff}, channel width W, substrate doping N_{sub}, and oxide thickness T_{OX}. Hence, there is a clear trade-off between the accuracy of the model and its complexity.

The behavior of the circuit is also predicted using the device model, and hence, the accuracy in the prediction of the circuit behavior depends upon the accuracy of the device model used in the circuit simulation. The circuit simulation (i.e., the prediction of the behavior of a circuit) may not be adequately accurate even if the device model used in the circuit simulation is highly accurate under the DC condition. The

various important requirements of the MOSFET model for incorporating it in a circuit simulator are discussed in the next section.

1.2 The Desirable Characteristics of a MOSFET Model Suitable for Analog Circuit Simulation

The device model is used for the bias point calculation in the circuit simulation as well as for calculating the small signal quantities such as the transconductance g_m (i.e., the ratio of the change in the drain current with respect to the change in the applied gate voltage), and the drain conductance g_d (i.e., the ratio of the change in the drain current with respect to the change in the applied drain voltage). All these small signal quantities along with the drain current should be continuous with respect to the terminal voltages. Several benchmark tests have been proposed by Tsividis and Suyama[3] for testing the performance of MOSFET models which can be used in analog circuit simulation. The characteristics which are to be exhibited by a MOSFET model in order to make it suitable for analog circuit simulation are briefly described below.

1. The model should account for the Drain Induced Barrier Lowering (DIBL) effect accurately. This effect is the lowering of the source-channel potential barrier in the subthreshold region due to the applied drain-to-source voltage in devices having very short channel lengths. This results in a considerable increase in the drain current in the subthreshold region of operation. It has negligible influence

in long channel MOSFETs, but ignoring this effect in the model development for short channel MOSFETs results in a large error in the subthreshold region drain current calculations.

2. In short channel devices, an increase in the drain voltage results in an increase in the subthreshold slope, where the subthreshold slope is the ratio of the change in the applied gate voltage to the change in the channel surface potential at the midpoint of the subthreshold region of operation, and hence, this affects the value of the drain current too in the subthreshold region. This is also a short channel effect which has to be considered in the model development in the subthreshold region.

3. The transconductance g_m becomes a constant in the strong inversion region (assuming that the I_D-V_{GS} characteristics can be expanded into a the first degree polynomial). On the other hand, in the weak inversion region, the drain current is dependent exponentially upon the applied gate voltage, and, hence, the ratio of the transconductance to the drain current (i.e., g_m/I_D) becomes a constant in the weak inversion region. This ratio, which is thus a constant in the weak inversion region, decreases as the device moves into the strong inversion region. This function (i.e., g_m/I_D) should be continuous with respect to V_{GS}. In many existing MOSFET models, this ratio becomes discontinuous in the moderate inversion region, i.e., at the boundary between the weak and the strong inversion regions. This is because the I_D-V_{GS} characteristic is neither exponential nor can be expressed by a first degree polynomial in the moderate inversion region[4].

The calculation of the transconductance in the moderate inversion region using either the strong or the weak inversion region model results in a large error. With the advent of low supply voltage designs, the moderate inversion region has become extremely important. The discontinuity in the transconductance results in a large error in the calculation of the gain of analog circuits. Thus, the continuity in g_m should be ensured in order to make the model suitable and accurate for analog circuit simulation.

4. The drain conductance g_d should be continuous with respect to the applied drain voltage V_{DS}. Most of the available models show an abrupt behavior of the drain conductance at the boundary between the linear and the saturation region. This abrupt behavior of g_d results in a large error in the gain calculation for analog circuits.

The continuities in the g_m/I_D ratio with respect to the applied gate voltage and that in g_d with respect to the applied drain voltage not only give accurate results in analog circuit simulation but also make the convergence in the simulation faster.

1.3 Literature Review

A brief overview of some recent MOSFET models is presented in this section. Also, the shortcomings of these models are highlighted.

The first MOSFET model, in which the DIBL effect was modeled by intro-

ducing a DIBL parameter δ was proposed by Troutman[5]. This DIBL parameter was purely a fitting parameter, and no analytical expression was given for it. Its value had to be found from the measurement data. It had been observed that δ was a function of the oxide thickness, the substrate doping, and the effective channel length. Thus, the DIBL effect was not adequately handled by this model.

The Berkeley Short Channel IGFET Model (BSIM)[6] is one of the most popular MOSFET models in recent times. This model is highly accurate, and it is partly physical and partly empirical, requiring quite a few fitting parameters. The subthreshold slope η in BSIM is given by the following equation[6]

$$\eta = \eta_o + \eta_B V_{SB} + \eta_D V_{DS}, \tag{1.1}$$

where η_o, η_B, and η_D are the model parameters, and the values of these parameters have to be found from the measurement data. No physical basis for η_o, η_B, and η_D are given. In the drain current model of BSIM, the strong inversion component has been matched with the weak inversion component at the boundary between the strong inversion and the weak inversion regions in order to restore the continuity in the drain current and its first derivative with respect to the applied gate voltage.

The Unified Charge Control Model (UCCM)[7] is a good model for analog circuit CAD (Computer Aided Design). It preserves the continuity in the derivatives of the drain current with respect to the terminal voltages at the various operating region boundaries. However, its major drawback is that it fails to predict the device behavior accurately in the deep subthreshold region, since it does not adequately model the effect of the applied drain voltage on the subthreshold slope for very short channel

The Physically based Continuous short-channel IGFET Model (PCIM)[8] is another analytical model for short channel devices. This model is described by a single drain current equation, valid for both the weak inversion and the strong inversion regions. This model maintains the continuity in the drain conductance as well as in the capacitances with respect to the terminal voltages at the various operating region boundaries. The DIBL effect has been modeled in this model. Since this model is based on the device physics, it automatically accounts for the changes in the behavior of the device with the changes in the device parameters such as the oxide thickness, substrate doping, temperature, and channel length. However it fails to model the behavior of the device in the deep subthreshold region.

A modified subthreshold slope model has been proposed by Kang et al.[9]. In this model, the values of the model parameters are determined from the threshold voltage data. This model adequately handles the DIBL effect by successfully expressing the subthreshold slope in terms of the threshold voltage parameters, after accounting for both the body and the DIBL effects. However, this model does not properly describe the effect of increase in the subthreshold slope with increase in the applied drain voltage. In order to develop a new and more accurate subthreshold slope model, this model[9] can be modified to make the subthreshold slope a function of the applied drain voltage. As mentioned before, the subthreshold slope equation in BSIM is purely empirical, where the values of the fitting parameters strongly depend upon the device specifications, such as T_{OX}, N_{sub}, L_{eff}, etc. This subthreshold slope model in BSIM can be replaced by the new subthreshold slope model developed in this work after

can be replaced by the new subthreshold slope model developed in this work after modifying the subthreshold slope model proposed by Kang et al.[9] in order to make BSIM more accurate.

1.4 A Brief Description of This Work

In this work, a new analytical model for the subthreshold slope has been developed. This model is strongly based on the device physics, and the subthreshold slope dependencies on the effective channel length, the body voltage V_{SB} and the applied drain voltage V_{DS} have been incorporated analytically into it along with the DIBL effect.

The subthreshold slope model proposed by Kang et al.[9] has been modified to come up with a new subthreshold slope model. The original subthreshold slope model[9] has been developed from the capacitor equivalent circuit of short channel MOSFETs in the subthreshold region of operation. In [9], the values of the capacitors in the circuit are analytically expressed in terms of the channel length after assuming that the parameters appearing in the expressions for the capacitances are independent of the drain voltage. Therefore the subthreshold slope in that model[9] becomes independent of the drain voltage. However, from the experimentally observed results, it has been observed that the subthreshold slope η is a strong function of the drain voltage, and it increases considerably with an increase in the drain voltage particularly for small channel length devices. Basically, in the subthreshold slope model proposed by Kang et al.[9], it was assumed that in the subthreshold region, the drain voltage

does not change the physical picture of the MOSFET channel depicted in terms of the capacitor equivalent circuit. However, it has been observed in this work that the point of the channel where the surface potential is minimum is a strong function of the drain voltage, the body voltage, and the effective channel length. This implies that, in the subthreshold region, the drain voltage, the body voltage, and the effective channel length modulate the values of the capacitors of the equivalent circuit given by Kang et al.[9]. This makes the subthreshold slope a function of these three parameters. We have analytically modeled the effects of these parameters on the minimum surface potential point, in order to develop an improved analytical subthreshold slope model which accounts for the dependencies of the subthreshold slope on the effective channel length, the drain voltage, and the body voltage.

In order to develop a drain current model, the subthreshold slope model and the threshold voltage model used in the drain current model developed by Deshpande and Dutta[10] have been replaced by the new subthreshold slope model developed in this work and the BSIM threshold voltage model respectively. The results of the improved subthreshold slope model and modified drain current model developed in this work have been compared with the experimentally obtained results reported in literature for MOSFETs having effective channel lengths ranging from 1.63 μm to 0.075 μm. The simulated results show a good match with the experimentally obtained ones.

1.5 The Organization of This Report

The development of the improved subthreshold slope model based on the BSIM threshold voltage model is discussed in detail in Chapter 2. This chapter also includes the development of the modified drain current model by replacing the subthreshold slope model and the threshold voltage model used in the drain current model developed by Deshpande and Dutta[10] by the improved subthreshold slope model developed in this work and the BSIM threshold voltage model respectively. The extraction procedure for the values of the various parameters used in the improved subthreshold slope model from the threshold voltage data is presented in Chapter 3. Also the simulated results of the improved subthreshold slope model and the drain current model have been presented in this chapter. The results from the experimentally obtained data for various short channel MOSFETs have been given along with the simulated results obtained from our model for the sake of comparison. The results show an excellent match. The summary of the entire work has been presented in Chapter 4 along with the conclusions. Also, the shortcomings of this model along with the future scope for improvement have been discussed in this chapter.

Chapter 2

Model Development

2.1 The MOSFET Structure

The basic three dimensional structure of an n-channel MOSFET is shown in Fig.2.1, along with the axes chosen. The channel length is along the x-direction, and the channel width is along the z-direction. The two n^+ regions (typically few tenths of a μm deep), which are diffused in the p-type substrate (or body) are called the source and the drain; and the inversion layer, which is formed in between these two regions is generally referred to as the channel. The structure also has a very thin layer of oxide (SiO_2) grown on the p-type substrate. The oxide thickness is denoted by T_{OX}, and it is typically several hundreds of $\mathring{A}$. The oxide is followed by a gate material (shown by the shaded region in the figure), which can be either metal or polysilicon. The drawn gate

length L is the length of the oxide which separates the n^+ drain and source diffusions. This is also known as the metallurgical channel length. When the drain and the source are actually diffused into the substrate, the effective channel length L_{eff} becomes less than the drawn length due to the lateral diffusion of the drain and the source dopants. The dashed line in the figure is the depletion region, whose width along the y-direction is referred to as X_{dep}. Obviously, this depletion width is a function of position along the length of the channel.

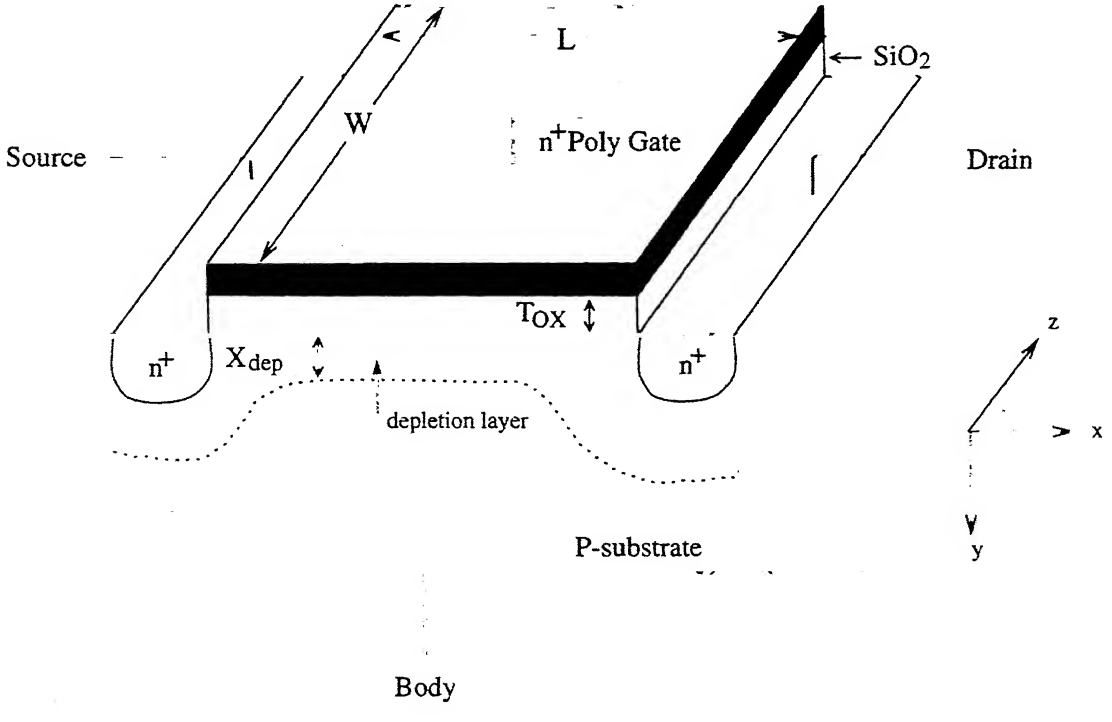


Figure 2.1: The Structure of an n-MOSFET.

2.2 The Subthreshold Slope Models

Theoretically, the subthreshold slope represents the changes in the surface potential ψ_s with respect to the applied gate voltage V_{GS} in the subthreshold region of operation. Also, the threshold voltage depends upon the surface potential variation with respect to the gate voltage. The changes in the geometry of the MOSFET, the substrate doping N_{sub}, and the oxide thickness T_{OX} affect the surface potential variation with respect to the gate voltage. This, in turn, affects the value of the subthreshold slope and the threshold voltage. Therefore, accurate subthreshold slope modeling is closely related to precise threshold voltage modeling. Actually, the subthreshold slope model can be developed from an accurate threshold voltage model.

2.2.1 The Classical Subthreshold Slope Model

A brief introduction to the classical subthreshold slope model[9] is given here. The various parameters used in this model are obtained from the threshold voltage data. The basic definition of the subthreshold slope or the ideality factor η is given by [11]

$$\eta = \frac{\delta V_{GS}}{\delta \psi_s}, \tag{2.1}$$

where V_{GS} is the gate-to-source voltage (henceforth referred to as the gate voltage), and ψ_s is the surface potential.

The ideality factor for long channel MOSFETs can be represented by[5]

$$\eta = 1 + \frac{C_B}{C_{OX}}, \tag{2.2}$$

where C_B is the depletion capacitance per unit area, and C_{OX} is the oxide capacitance per unit area.

It has been found that for long channel devices, the results obtained from this model match well with the measurement results [5]. However, this model cannot be used for short channel devices due to various second-order effects. For such devices, the ideality factor model has to properly consider the various short channel effects.

For short channel MOSFETs, the threshold voltage V_{Ts} is given by [6]

$$V_{Ts} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}} - \Gamma(2\phi_F + V_{SB}) - \sigma V_{DS}, \tag{2.3}$$

where V_{FB} is the flat band voltage, ϕ_F is the bulk potential, V_{SB} is the applied source-to-body voltage (henceforth referred to as the body voltage), V_{DS} is the applied drain-to-source voltage (henceforth referred to as the drain voltage), γ is the body effect coefficient, Γ is the nonuniform doping effect parameter, and σ is the Drain-Induced Barrier Lowering (DIBL) parameter.

Since the subthreshold slope η is defined as $\left(\frac{\delta\psi_s}{\delta V_{GS}}\right)^{-1}$, from Eqns.(2.2) and (2.3), the expression for $\frac{C_B}{C_{OX}}$ can be obtained by substituting V_{GS} for V_{Ts}, ψ_s for $2\phi_F$, and taking the derivative of V_{GS} with respect to ψ_s. Thus, $\frac{C_B}{C_{OX}}$ can classically be expressed as [11]

$$\frac{C_B}{C_{OX}} = \frac{\gamma}{2\sqrt{1.5\phi_F + V_{SB}}} - \Gamma. \tag{2.4}$$

Thus, from Eqns.(2.2) and (2.4), the classical model of the subthreshold slope η can be given by

$$\eta = 1 + \frac{\gamma}{2\sqrt{1.5\phi_F + V_{SB}}} - \Gamma. \tag{2.5}$$

It should be noted that the DIBL effect, which is extremely important for short channel MOSFETs, has been neglected in this model [Eqn.(2.5)]. In this work, an analytical subthreshold slope model is developed taking into account the DIBL effect in a comprehensive manner.

2.2.2 The DIBL Effect

In the subthreshold region, there is a capacitive coupling present between the channel and the source/drain, which can be represented by two coupling capacitances C_{SC} and C_{DC} respectively. These capacitances are in addition to the already existing capacitances C_{OX} and C_B, and are given by

$$C_{SC} = \frac{\epsilon_{si} k}{x_o}, \tag{2.6}$$

and

$$C_{DC} = \frac{\epsilon_{si} k}{L_{eff} - x_o}, \tag{2.7}$$

where ϵ_{si} is the permittivity of Si, k is the proportionality constant, L_{eff} is the effective channel length, and x_o is the distance along the channel (measured from the source) where the surface potential is minimum. Thus, the equivalent circuit of a short channel MOSFET at subthreshold can be given as shown in Fig.2.2.

Therefore, the surface potential changes not only due to the gate voltage V_{GS}

but also due to the drain voltage V_{DS}. The parameter σ appearing in Eqn.(2.3) models this effect. The values of these coupling capacitances (C_{DC} and C_{SC}) increase as the channel length is reduced. The value of the DIBL parameter σ also increases as the channel length is reduced, which implies that the DIBL effect is more pronounced in short channel MOSFETs. This makes it important to model this effect accurately with the help of the parameter σ. This parameter is a function of the effective channel

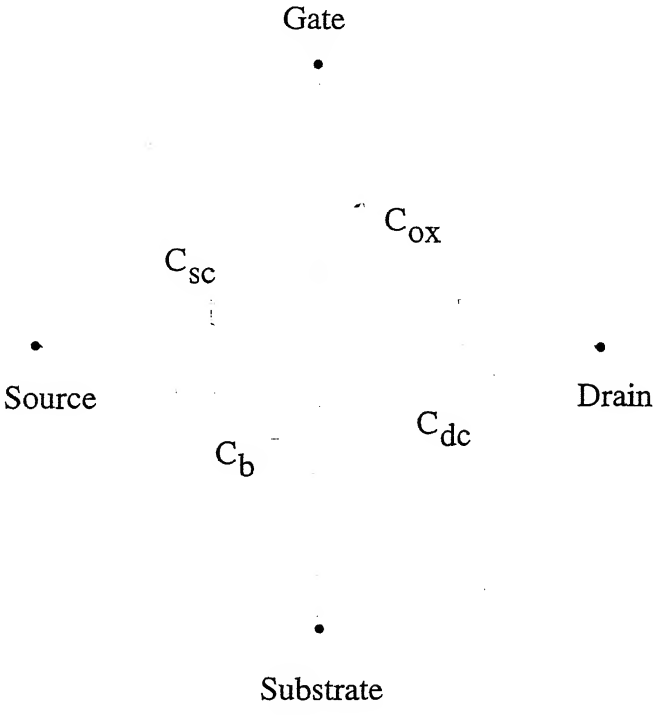


Figure 2.2: Capacitor equivalent circuit of a short channel MOSFET at subthreshold.

length L_{eff} and the body voltage V_{SB}. In order to find the variation in the value of σ with respect to the term $\sqrt{2\phi_F} + V_{SB}$ for a particular channel length, $\Delta V_{Ts}/\Delta V_{DS}$ (i.e., the change in the threshold voltage V_{Ts} with respect to the change in the drain voltage V_{DS}) can been plotted with respect to $\sqrt{2\phi_F} + V_{SB}$ for that particular channel length.

Figure 2.3 shows the plots of $(\Delta V_{Ts}/\Delta V_{DS})/\sqrt{2\phi_F + V_{SB}}$ as a function of $\sqrt{2\phi_F + V_{SB}}$ for four different values of the effective channel lengths (i.e., for $L_{eff} = 0.33$ μm, 0.43 μm, 0.63 μm, and 1.43 μm). These data are obtained from the results reported by Lee and Min[13]. From this plot, the values of σ can be obtained for various channel lengths. These results are described in the next chapter.

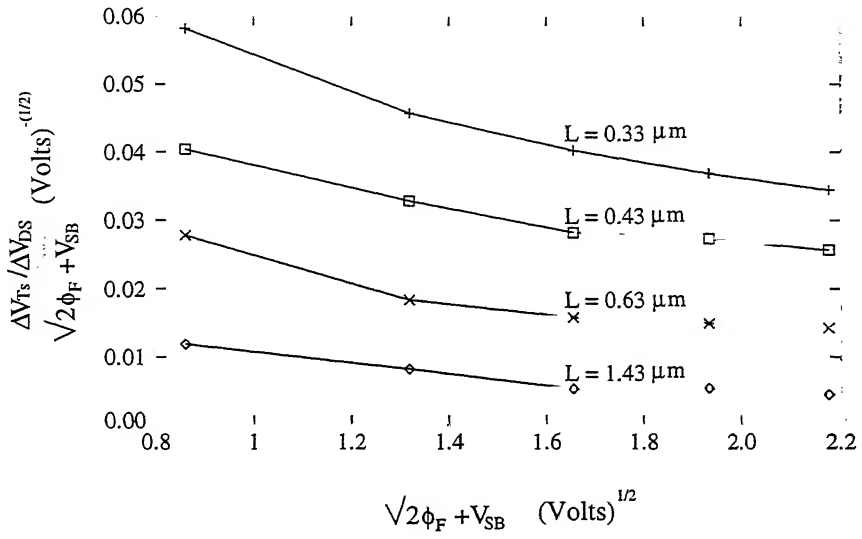


Figure 2.3: $(\Delta V_{Ts}/\Delta V_{DS})/(2\phi_F + V_{SB})^{1/2}$ versus $(2\phi_F + V_{SB})^{1/2}$ for different channel lengths.

The DIBL parameter σ has been expressed as [9]

$$\sigma = s\sqrt{2\phi_F + V_{SB}} - S(2\phi_F + V_{SB}), \tag{2.8}$$

where s and S are the model parameters, which are used to model the behavior of σ with respect to V_{SB}. Thus, one can obtain the values of γ, Γ, s and S by the method of curve fitting on the threshold voltage data. The results obtained from this type of

parameter extraction are described in the next chapter.

The channel potential can be calculated by the capacitance-coupling theory as [9]

$$\psi_s = \psi_{s0}(V_{G0}, V_{SB}, V_{S0}, V_{D0}) + \frac{C_{OX}(V_G - V_{G0}) + C_{SC}(V_S - V_{S0}) + C_{DC}(V_D - V_{D0})}{C_{OX} + C_B + C_{DC} + C_{SC}}. \tag{2.9}$$

In Eqn.(2.9), ψ_s has been expressed by expanding the Taylor series around ψ_{s0} = $1.5\phi_F + V_{SB}$ (which is the approximate middle point of the subthreshold region), and keeping only the first-order terms. Since the corrections in the values of V_{Ts} and η due to the capacitances C_{DC} and C_{SC} are quite small, it is enough to keep only the first-order terms in the Taylor series expansion.

2.2.3 The Subthreshold Slope Considering the DIBL Effect

The ideality factor η is obtained by partial differentiation of Eqn.(2.9) with respect to V_G, and it can be expressed as [9]

$$\eta = 1 + \frac{C_B + C_{SC} + C_{DC}}{C_{OX}},$$

or

$$\eta \approx 1 + \frac{C_B}{C_{OX}} + \frac{2C_{DC}}{C_{OX}}. \tag{2.10}$$

In obtaining Eqn.(2.10), the subthreshold slope η is evaluated at $V_{DS} = 0$, and, therefore, the capacitances C_{SC} and C_{DC} have the same value, since the minimum surface potential point is located at the middle of the channel, i.e., at $x_o = L_{eff}/2$. Thus, from Eqns.(2.6) and (2.7), one gets

$$C_{DC}(V_{DS} = 0) = C_{SC}(V_{DS} = 0) = 2\epsilon_{Si}k/L_{eff}. \tag{2.11}$$

By partial differentiation of Eqn.(2.9) with respect to V_{DS}, and neglecting C_{DC} and C_{SC} terms appearing in the denominator, the following relationship can be obtained [9]

$$\sigma = \frac{C_{DC}}{C_B + C_{OX} + C_{DC} + C_{SC}},$$

or

$$\sigma \approx \frac{C_{DC}}{C_B + C_{OX}}. \tag{2.12}$$

The term C_{DC} appearing in Eqn.(2.12) is the drain-channel coupling capacitance for large values of V_{DS} [9]. From Eqn.(2.7), it can be clearly seen that C_{DC} is inversely proportional to $L_{eff} - x_o$. Though the minimum surface potential point x_o is known to be a complex function of the channel length, the oxide thickness, and the drain voltage [14], it has been stated that for large values of V_{DS}, it becomes independent of V_{DS} and converges rapidly to a value equal to $L_{eff}/3$ [15]. Therefore, for large values of V_{DS}, C_{DC} can be expressed as [9]

$$C_{DC}(large\ V_{DS}) = \frac{3\epsilon_{Si}k}{2L_{eff}}. \tag{2.13}$$

Thus, from Eqns.(2.11) and (2.13), one can write

$$C_{DC}(V_{DS} = 0) = \frac{4C_{DC}(large\ V_{DS})}{3}. \tag{2.14}$$

Similarly, from Eqns.(2.12) and (2.14), one gets

$$C_{DC}(V_{DS} = 0) = \frac{4\sigma(C_B + C_{OX})}{3}. \tag{2.15}$$

Thus, from Eqns.(2.4), (2.10), and (2.15), one gets the final expression for the ideality factor, which is given by [9]

$$\eta = \left(1 + \frac{\gamma}{2\sqrt{1.5\phi_F + V_{SB}}} - \Gamma\right)(1 + 2.7\sigma). \tag{2.16}$$

In this derivation, it has been assumed that the minimum surface potential point lies at a distance equal to $L_{eff}/3$ from the source. This assumption makes the ideality factor independent of V_{DS}, which is incorrect, as has been proved by the experimental data on short channel length devices reported in literature, which show changes in the subthreshold slope η with a change in the applied drain voltage V_{DS}.

The development of the improved subthreshold slope model considering the effect of the applied drain voltage V_{DS} is described in the following section.

2.2.4 The Improved Subthreshold Slope Model

This section describes the simulation algorithm, which accounts for the dependence of η on V_{DS}. In reality, the minimum surface potential point x_o is a function of V_{DS} and L_{eff}. Thus, if these variations can be modeled in the expression for x_o, then the expressions for C_{DC} and C_{SC} would also be altered, with each having a specific dependence on V_{DS} and L_{eff}. And since η is a function of C_{DC} and C_{SC}, it will have an explicit dependence on V_{DS} and L_{eff}, which previous authors have failed to model.

The algorithm is as follows.

1. Evaluate the surface potential at each point of the channel for various values of L_{eff} and V_{DS}.

2. Find the values of x_o (i.e., the distance of the minimum surface potential point from the source) for different values of L_{eff} and V_{DS}.

3. Use these values of x_o (having strong dependence on V_{DS} and L_{eff}) for finding the values of C_{DC} and C_{SC}.

4. Then, compute η as a function of V_{DS} and L_{eff} from the expression given earlier.

The details are given below.

The built-in voltage of the source-substrate junction is given by

$$V_{bi} = V_T \, ln \left(\frac{N_{sub} N_D}{{n_i}^2} \right), \tag{2.17}$$

where V_T is the thermal voltage (= kT/q), N_{sub} and N_D are the substrate and the source doping concentrations respectively, and n_i is the intrinsic carrier concentration. The depletion layer thickness at the source end (at threshold) is given by [11]

$$X_{dep} = \sqrt{2\epsilon_{si}(2\phi_F + V_{SB})/qN_{sub}}. \tag{2.18}$$

The surface potential $\psi_s(x)$ as a function of V_{DS} and L_{eff} (at $V_{SB} = 0$) can be given by [14]

$$\psi_s(x) = \psi_{sL} + (V_{bi} + V_{DS} - \psi_{sL}) \frac{sinh(x/l)}{sinh(L/l)} + (V_{bi} - \psi_{sL}) \frac{sinh[(L-x)/l]}{sinh(L/l)}, \tag{2.19}$$

where ψ_{sL} is the long channel surface potential, given by [14]

$$\psi_{sL} = V_{GS} - V_{th0} + 2\phi_F, \tag{2.20}$$

with V_{th0} being the long channel threshold voltage, given by[14]

$$V_{th0} = V_{FB} + \frac{qN_{sub}X_{dep}T_{OX}}{\epsilon_{OX}} + 2\phi_F, \tag{2.21}$$

where T_{OX} is the oxide thickness, and ϵ_{OX} is the permittivity of the oxide. The characteristics length l is defined by [14]

$$l = \sqrt{\frac{\epsilon_{si}T_{OX}X_{dep}}{\epsilon_{OX}\eta_f}}. \tag{2.22}$$

The depletion layer thickness X_{dep} at threshold has been assumed to be uniform along the channel. However, in reality, it is a function of V_{DS} and L_{eff}, particularly so for short channel length devices. Therefore, in order to compensate for this invalid assumption (of constant X_{dep}), another factor η_f has been introduced in the expression for l [Eqn.(2.22)], which is basically a fitting parameter called as the fudge factor. X_{dep}/η_f may be taken as an average of the depletion layer thickness along the channel. The fudge factor η_f itself may be a function of V_{DS}, however this is a second order effect, and hence it is neglected [14].

It has been observed that for long channel devices in subthreshold, the surface potential is almost constant throughout the channel. Hence, the value of η_f can be taken to be equal to unity. However, for short channel devices (having submicron channel lengths), the portion of the channel where the surface potential stays constant is quite small, and, hence, the value of η_f is correspondingly higher. From the

And finally, the improved expression for the ideality factor developed in this work can be given by

$$\eta = \left(1 + \frac{\gamma}{2\sqrt{1.5\phi_F + V_{SB}}} - \Gamma\right)\left(1 + 4(1 - \frac{x_o}{L_{eff}})\sigma\right). \tag{2.26}$$

Equation (2.26) is the improved subthreshold slope model developed in this work, and will be used for estimating the subthreshold region drain current, as illustrated in the next section. The results are presented in the next chapter.

2.3 The Subthreshold Region Drain Current Model

The subthreshold region drain current expression for a short channel MOSFET is given by [10]

$$I_D = \frac{W}{L_{eff}} \mu_n {V_T}^2 \frac{\sqrt{2q\epsilon_{si}N_{sub}(2\phi_F + V_{SB})}}{2\psi^0}(1 - e^{-\beta V_{DS}})e^{\beta(V_{GS} - V_{Ts})/\eta}, \tag{2.27}$$

where μ_n is the electron mobility, ψ^0 is the short channel surface potential given by [10]

$$\psi^0 = V_{GS} - V_{th0} + 2\phi_F + V_{SB}, \tag{2.28}$$

V_{th0} is the long channel threshold voltage [Eqn.(2.21)], V_{Ts} is the short channel threshold voltage [Eqn.(2.3)], β is the reciprocal of the thermal voltage V_T, and η is the subthreshold slope [Eqn(2.26)].

2.4 The Strong Inversion Region Drain Current Model

The strong inversion region drain current model is given by Sheu et al.[6]. This model has been modified by Deshpande and Dutta[10]. The modification algorithm of Deshpande and Dutta[10] is briefly reproduced here. The strong inversion component of the drain current I_{lin} in the linear region is given by [6]

$$I_{lin} = \frac{W}{L_{eff}} C_{OX} \frac{\mu_n}{1 + \theta V_{DS} + U_0 V_{GT}} \frac{(V_{GT} V_{DS} - \frac{\alpha'}{2} V_{DS}^2)}{(1 + \frac{U_1}{L_{eff}} V_{DS})}, (V_{GT} > 0, 0 < V_{DS} < V_{DSAT}) \tag{2.29}$$

where[4]

$$V_{GT} = V_{GS} - V_{Ts}, \tag{2.30}$$

$$\alpha' = 1 + \frac{g\gamma}{2\sqrt{2\phi_F + V_{SB}}}, \tag{2.31}$$

and

$$g = 1 - \frac{1}{1.744 + 0.8364(2\phi_F + V_{SB})}, \tag{2.32}$$

U_0 is the vertical field mobility degradation coefficient, U_1 is the velocity saturation coefficient, and θ accounts for the source and drain parasitic series resistances [6].

The parameters γ and Γ model the non-uniform doping profile [4]. In addition to modeling the DIBL effect, the parameter σ accounts for the channel length modulation effect as well[6].

The drain current expression in the saturation region ($V_{GS} > V_{Ts}$, and $V_{DS} \geq V_{DSAT}$) is given by [6]

$$I_{sat} = \frac{W}{L_{eff}} C_{OX} \frac{\mu_n}{1 + \theta V_{DS} + U_0 V_{GT}} \frac{{V_{GT}}^2}{2\alpha' K}, \tag{2.33}$$

where

$$K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2}, \tag{2.34}$$

with

$$v_c = \frac{U_1}{L_{eff}} \frac{V_{GT}}{\alpha'}. \tag{2.35}$$

The drain-to-source saturation voltage V_{DSAT} is given by [6]

$$V_{DSAT} = \frac{V_{GT}}{\alpha' \sqrt{K}}. \tag{2.36}$$

An additional parameter l_1 had been introduced by Deshpande and Dutta[10] in order to take into account the channel length modulation effect in the saturation region drain current expression, with the final expression given by [10]

$$I'_{sat} = \frac{W}{L_{eff}} C_{OX} \frac{\mu_n}{1 + \theta V_{DS} + U_o V_{GT}} \frac{V_{GT}^2}{2\alpha' K(1 - l_1(V_{DS} - V_{DSAT}))}. \tag{2.37}$$

However, the DIBL parameter σ partially accounts for the channel length modulation effect [6]. Therefore, the threshold voltage model [Eqn.(2.3)] used here already accounts for this effect. Hence, one need not incorporate the parameter l_1 separately for it. Therefore, Eqns.(2.27), (2.29), and (2.33) give the expressions for the drain currents for subthreshold, linear and saturation regions respectively.

2.5 Approaches for Joining the Various Regions of Operations of the MOSFET

The discontinuities in the drain current (I_D), the drain conductance (g_d), and the transconductance (g_m) with respect to the terminal voltages at the boundaries between the various regions of operation create large errors in circuit simulation, especially for analog circuits [3]. The most basic requirement for a MOSFET model fit to be used in analog circuit simulation work is the continuity of I_D versus V_{GS} characteristics. The discontinuities occur at two points in the operating range, one at the boundary between the weak and the strong inversion regions (i.e., at $V_{GS} = V_{Ts}$), and the other at the boundary between the linear and the saturation regions (i.e., at $V_{DS} = V_{DSAT}$).

The discontinuity of I_D with respect to V_{GS} at the onset of strong inversion is due to a total disappearance of the strong inversion component of I_D in the weak inversion region (i.e., for $V_{GS} < V_{Ts}$). The improper models used for the weak and the strong inversion regions can also lead to a discontinuity in I_D with respect to V_{GS} at the boundary between the weak and the strong inversion regions [3]. The discontinuity in the derivative of I_D with respect to V_{DS} occurs at the boundary between the linear and the saturation regions. In the saturation region ($V_{GS} > V_{Ts}$, and $V_{DS} > V_{DSAT}$), I_D is almost constant with respect to V_{DS} (neglecting the channel length modulation effect) with a value almost equal to that obtained for $V_{DS} = V_{DSAT}$, whereas in the linear region ($V_{GS} > V_{Ts}$, and $V_{DS} < V_{DSAT}$), I_D varies almost linearly with V_{DS}. This abrupt change of characteristic for I_D from the linear to the saturation region makes

the derivative of I_D discontinuous with respect to V_{DS}.

2.6 Continuity in the Drain Conductance with Respect to the Drain Voltage

As mentioned before, the discontinuity in the drain conductance (g_d) with respect to the applied drain voltage V_{DS} arises at the boundary between the linear and the saturation regions. The drain current I_D is a strong function of the drain voltage V_{DS} in the linear region, whereas in the saturation region, it becomes essentially constant. This implies that the drain current I_D has completely different dependencies on the drain voltage V_{DS} in these two regions. This change in the behavior of I_D with respect to V_{DS} occurs at the boundary between the linear and the saturation regions, and it is abrupt. Therefore, V_{DS} can be viewed as if it saturates to V_{DSAT} in an abrupt manner at the onset of saturation (i.e., at $V_{DS} = V_{DSAT}$). In order to remove this discontinuity, Deshpande and Dutta[10] have made V_{DS} approach V_{DSAT} gradually. This has been accomplished by replacing V_{DS} in Eqn.(2.29) by "effective drain-to-source voltage V_{dsx}". The expression for V_{dsx} is given by [10]

$$V_{dsx} = V_{DSAT}\left(1 + \frac{ln[1 + exp(A(1 - \frac{V_{DS}}{V_{DSAT}}))]}{ln[1 + exp(A)]}\right), \tag{2.38}$$

where the coefficient A is a fitting parameter, and the sharpness in the transition of V_{dsx} to V_{DSAT} depends on its value.

Equation (2.38) has been simulated and plotted in Fig.2.4, which clearly shows that the value of V_{dsx} gradually approaches V_{DSAT} beyond the point $V_{DS} = V_{DSAT}$. In the linear region, the value of V_{dsx} is almost equal to the value of V_{DS}. The behavior of V_{dsx} around the transition point (i.e., at $V_{DS} = V_{DSAT}$) depends upon the value of A. From Fig.2.4, the effects of the value of A on the transition of the curve can be observed. For curves having sharp transitions, the values of A are high, whereas for gradually changing curves, the values of A are low. It has been observed that for very short channel devices, the value of A is low because of the widening in the transition width [10]. The width of the transition from the linear to the saturation region is low for long channel devices, therefore the value of A is correspondingly higher.

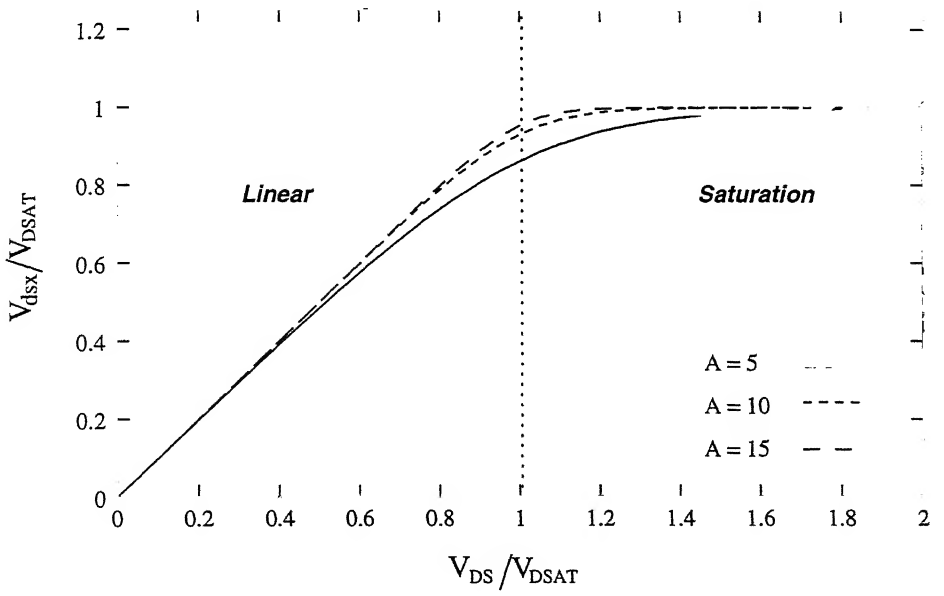


Figure 2.4: The normalized effective drain-to-source voltage (V_{dsx}/V_{DSAT}) versus the normalized applied drain-to-source voltage (V_{DS}/V_{DSAT}) for various values of A.

From Eqns.(2.29) and (2.38), a single expression has been derived by Deshpande and Dutta [10] for the strong inversion region drain current, which can be given by

$$I_{str} = \frac{W}{L_{eff}} C_{ox} \frac{\mu_n}{(1+\theta V_{DS}+U_0 V_{GT})} \frac{V_{GT}V_{dsx} - \frac{\alpha'}{2}V_{dsx}^2}{(1+\frac{U_1}{L_{eff}}V_{dsx})}. \tag{2.39}$$

Equation (2.39) maintains the continuity of the drain conductance with respect to the applied drain voltage V_{DS} at the boundary between the linear and the saturation region. These results are shown in the next chapter.

2.7 Continuity in the Transconductance (g_m) with Respect to the Gate Voltage

The transconductance (g_m) should be continuous with respect to V_{GS} at various operating region boundaries. Discontinuity in g_m occurs at the boundary between the weak and the strong inversion regions (i.e., at $V_{GS} = V_{Ts}$). This discontinuity is removed by Deshpande and Dutta [10] by making the weak inversion component of the drain current slowly saturate to some value as V_{GS} is increased beyond V_{Ts}. This is accomplished by modifying the weak inversion component of the drain current as [10]

$$I'_{sub} = \frac{\hat{I}_{sub}\, I_{limit}}{\hat{I}_{sub} + I_{limit}}, \tag{2.40}$$

where the term $\hat{I}_{sub}$ is given by [10]

$$\hat{I}_{sub} = M \frac{W}{L_{eff}} \mu_n {V_T}^2 \sqrt{\frac{2q\epsilon_s N_{sub}(2\phi_F + V_{SB})}{2\psi^o}} (1 - e^{-\beta V_{DS}}) e^{\beta(V_{GS}-V_{Ts})/\eta}, \tag{2.41}$$

where M is a fitting parameter, which is used to describe the moderate inversion region. and the value of this parameter is empirically chosen to achieve best fits in the subthreshold region characteristics with minimum effect on the strong-inversion region characteristics [6]. I_{limit} is given by [10]

$$I_{limit} = \hat{I}_{sub}|_{V_{GT}=0}. \tag{2.42}$$

The higher order continuity in the transconductance with respect to the applied gate voltage V_{GS} is restored by Deshpande and Dutta [10] by making the strong inversion component I_{str} gradually decrease to zero as V_{GS} decreases below V_{Ts}. This gradually decreasing drain current component I_{str} in the weak inversion region should be much smaller than the actual weak inversion component. In order to accomplish this, the voltage V_{GT} is modified to an effective voltage V_{gtx} such that [10]

$$V_{gtx} = s_1 \, ln \left(1 + \frac{V_{GT}}{s_1}\right), \tag{2.43}$$

where s_1 is a fitting parameter. This equation has been simulated and the normalized values of V_{gtx} have been plotted in Fig.2.5 for two different values of the fitting parameter s_1 ($0.5V_T$ and V_T) as a function of the normalized values of V_{GT}. In the strong inversion region ($V_{GT} > 0$), V_{gtx} approaches V_{GT}. On the other hand, in the weak inversion region ($V_{GT} < 0$), the values of V_{gtx} are much less than V_{GT}. Thus, the behaviour of the V_{gtx} in the Fig.2.5 implies that the strong inversion component of the drain current in the weak inversion region holds some nonzero value which is much much less than the weak inversion component value.

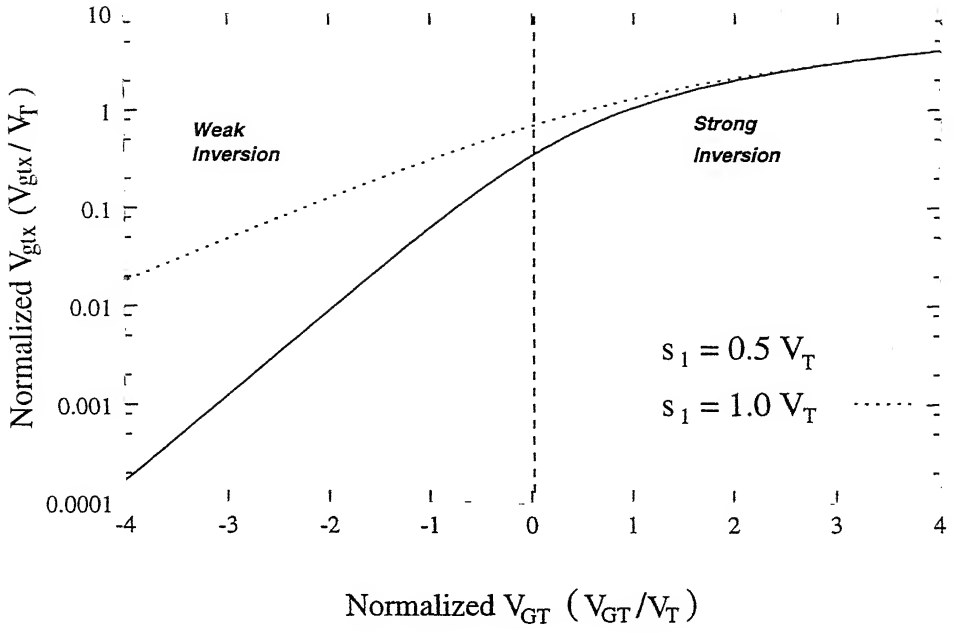


Figure 2.5: Normalized values of V_{gtx} for two different values of s_1 ($0.5V_T$ and V_T).

2.8 The Complete Model

The total drain current is the sum of the weak and the strong inversion components, which can be given by

$$I_D = I_{str}{}' + I_{sub}{}', \tag{2.44}$$

where $I_{str}{}'$ is the combined strong inversion component of the drain current, valid for both the linear and the saturation regions, given by [10]

$$I_{str}{}' = \frac{W}{L_{eff}} C_{ox} \frac{\mu_n}{(1+\theta V_{DS}+U_0 V_{gtx})} \frac{V_{gtx}V_{dsx} - \frac{\alpha'}{2}V_{dsx}^2}{(1+\frac{U_1}{L_{eff}}V_{dsx})}, \tag{2.45}$$

and the weak inversion component $I_{sub}{}'$ of the drain current is given by Eqn.(2.40).

The fitting parameters k', s_1, θ, U_0, U_1, A, μ_n, γ, Γ, σ, η_{fo} are to be extracted from the measurement data. The parameters σ, γ and Γ can be extracted from the threshold voltage data. The values of the parameters η_{fo} and k' are to be extracted from the measurement data of the subthreshold slope. The results simulated from this model are given in the next chapter.

Chapter 3

Model Results

In this chapter, the simulated results of the models described in the previous chapter are presented. Initially, the simulated results for the subthreshold slope model described by Kang et al.[9] are presented, and the inherent flaws in that model are highlighted. Next, the simulated results of the improved subthreshold slope model developed in this work are presented. The parameters required for this model are extracted from the threshold voltage data. The current-voltage characteristics simulated from this improved model are also given. The model results are compared with the experimental data reported in literature for devices having channel lengths less than hundred nanometers, and the results show a good match.

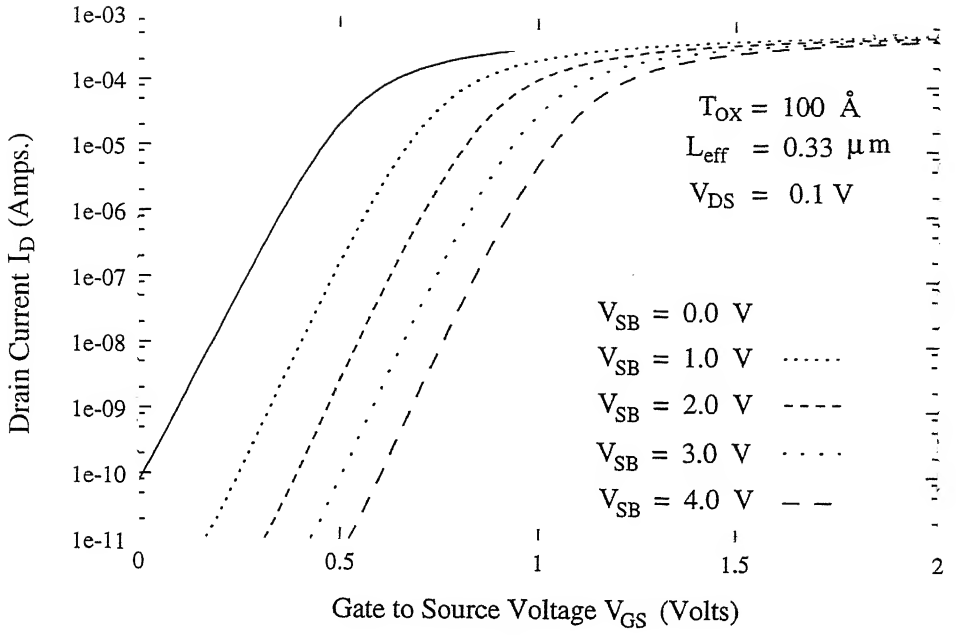
3.1 Simulation Results of the Subthreshold Slope Models

In this section, the simulated results of the subthreshold slope models described in the previous chapter are presented. For this simulation, MOSFETs having effective channel lengths of 1.43 μm, 0.63 μm, 0.43 μm, and 0.33 μm are considered. The oxide thickness is 100 $\AA$ and the substrate doping is 1.6×10^{17} per cm^3. We have the I_D versus V_{GS} characteristics for these devices for V_{SB} = 0, 1, 2, 3, and 4 V, and for V_{DS} = 0.1 V and 3.0 V[13]. These characteristics are plotted in Figs.3.1(a) and (b) for channel lengths of 0.33 μm and 0.63 μm respectively, for different values of the body voltage V_{SB}.

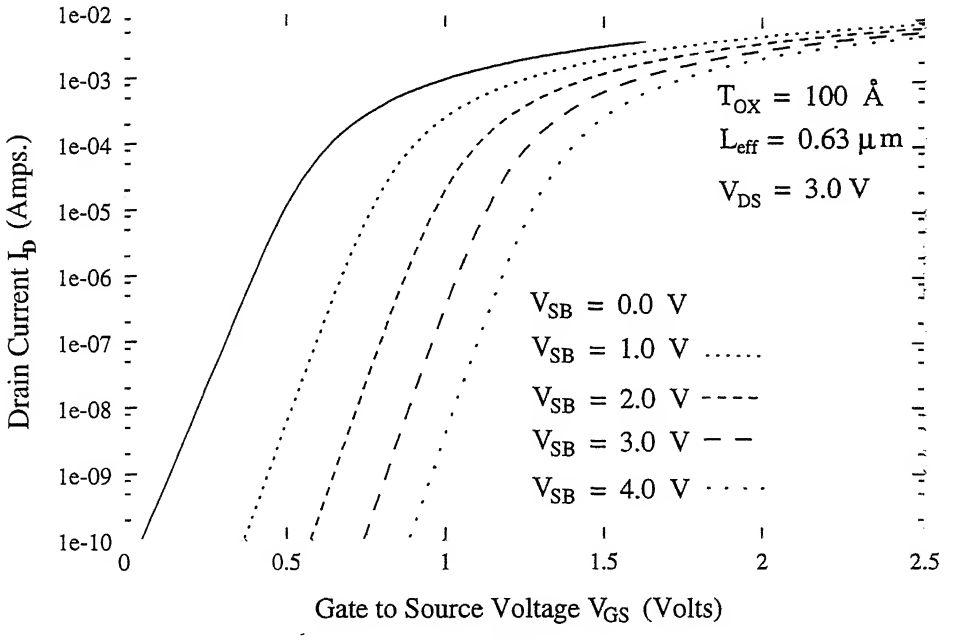
3.1.1 The Subthreshold Slope Model based on the Threshold Voltage Data (without considering the effect of V_{DS} on η)

In this section, the method of extraction of the values of the parameters s, S, γ, and Γ from the threshold voltage data for the four devices having different channel lengths are presented. From these parameters, the values for the subthreshold slope are determined from Eqn.(2.16). This model for the subthreshold slope is independent of V_{DS}, as explained in the previous chapter.

In order to obtain the values of the parameters s and S, the term



(a)



(b)

Figure 3.1: Experimentally obtained I_D-V_{GS} characteristics of the MOSFETs having effective channel lengths of (a) $L_{eff} = 0.33\,\mu m$ and (b) $L_{eff} = 0.63\,\mu m$[13].

$(\triangle V_{Ts}/\triangle V_{DS})/\sqrt{2\phi_F} + V_{SB}$ has been plotted as a function of $\sqrt{2\phi_F} + V_{SB}$ in Fig.2.3. The term $\triangle V_{Ts}$ is defined as[6]

$$\triangle V_{Ts} = V_{Ts}(V_{DS} = 0.1\,V) - V_{Ts}(V_{DS} = 3.0\,V). \tag{3.1}$$

The threshold voltage V_{Ts} for $V_{DS} = 0.1$ V has been obtained by using the following rule of thumb[7,11]

$$V_{Ts\ (V_{DS}=\ 0.1\,V)} = V_{GS\ (g_m = g_{mmax}/3)}, \tag{3.2}$$

where the term g_m is the transconductance, defined as the first derivative of I_D with respect to V_{GS}, given by

$$g_m = \frac{\delta I_D}{\delta V_{GS}}, \tag{3.3}$$

and $g_{m_{max}}$ is the maximum value of g_m. The g_m versus V_{GS} characteristics have been plotted in Figs.3.2(a) and (b). From these figures, it can be observed that proper maxima exist for $V_{DS} = 0.1$ V, but no such maxima exist for $V_{DS} = 3$ V. This is due to the saturation effect which occurs for $V_{DS} = 3$ V. In saturation, the transconductance g_m varies almost linearly with the applied gate voltage V_{GS}. Therefore, due to this effect, the method given in Eqn.(3.2) for obtaining V_{Ts} can not be applied for $V_{DS} =$ 3 V. Hence, for these cases, the values of V_{Ts} have been obtained from the method of constant current threshold voltage, given by [11,12]

$$V_{Ts}\,|_{V_{DS}=3.0\ V} = V_{GS}|_{I_D = 5\,\mu A}, \tag{3.4}$$

where $I_D = 5\ \mu$A is chosen to be the reference value for the drain current.

As stated by Kang et al.[9], for relatively longer channel MOSFETs (e.g., for

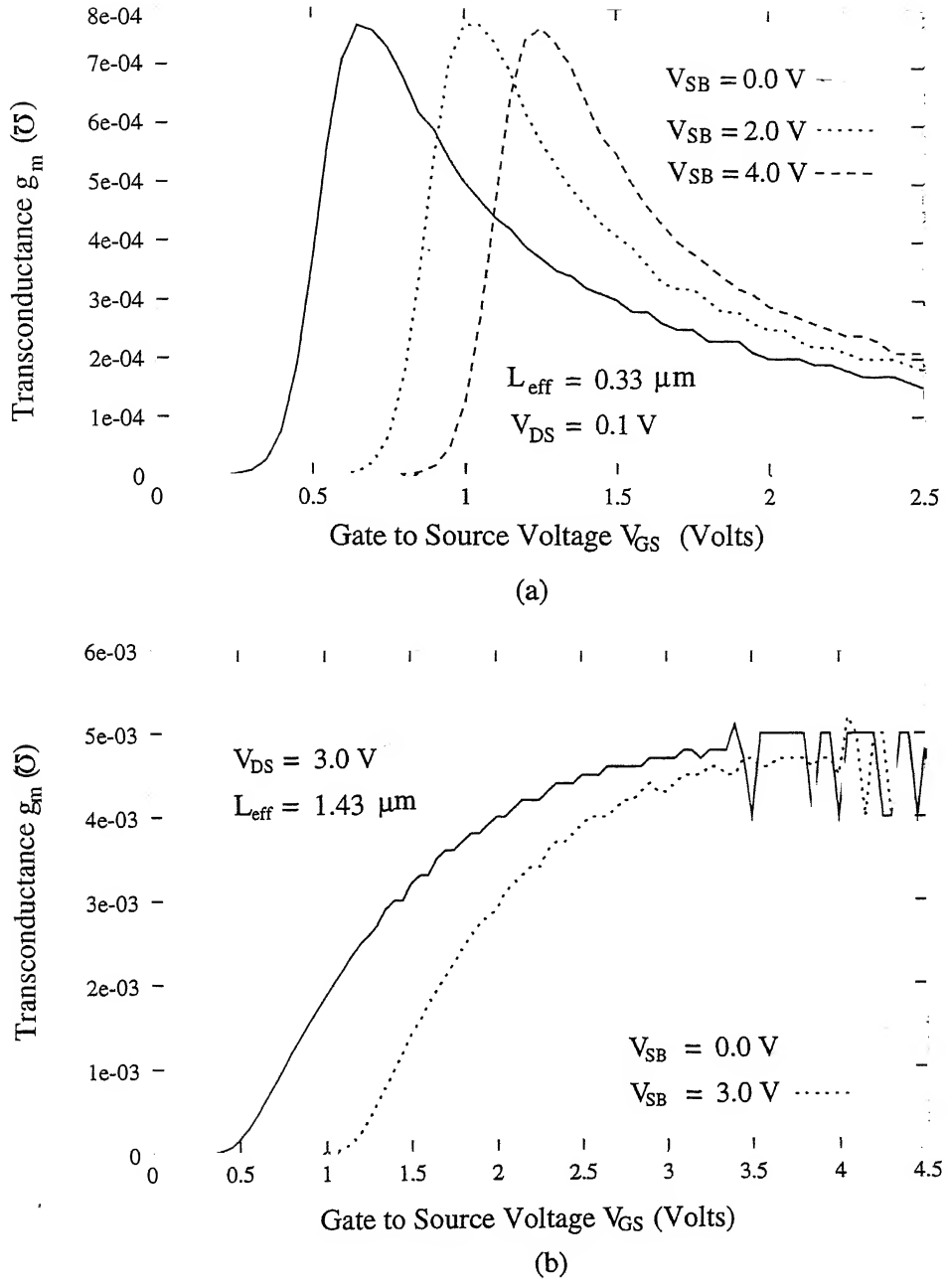


Figure 3.2: Transconductance g_m versus V_{GS} for (a) $L_{eff} = 0.33$ μm and $V_{DS} = 0.1$ V and (b) $L_{eff} = 1.43$ μm and $V_{DS} = 3.0$ V.

$L_{eff} = 1.43$ μm), the term $(\triangle V_{Ts}/\triangle V_{DS})/\sqrt{2\phi_F + V_{SB}}$ is observed to be almost constant, independent of $\sqrt{2\phi_F + V_{SB}}$. It indicates that $\triangle V_{Ts}/\triangle V_{DS}$ is directly proportional to the factor $\sqrt{2\phi_F + V_{SB}}$ in such MOSFETs. It can be observed from Eqn.2.3 that the factor $\triangle V_{Ts}/\triangle V_{DS}$ has the same functional behavior as that of σ. The factor $\triangle V_{Ts}/\triangle V_{DS}$ has been modeled by the expression given by Eqn.(2.8). The values of the parameters s and S have been obtained from curve fitting of Eqn.(2.8) with Fig.2.3. It has been observed that the value of s (and ultimately that of σ) increases as the channel length is reduced. This implies that the drain-induced barrier lowering effect becomes more pronounced as the channel length is reduced. The behavior of $\triangle V_{Ts}$ follows the same pattern as suggested by Liu et al.[14].

The values of the parameters γ and Γ have been found by curve fitting of Eqn.(2.3) with the V_{Ts} data for $V_{DS} = 0.1$ V. The extracted values of the model parameters γ, Γ, s, and S are listed in Table 3.1, and they match well with those reported by Kang et al.[9]. These extracted values of the model parameters γ, Γ, s, and S are used in Eqn.(2.16) in order to calculate the ideality factor η as a function of V_{SB}. These characteristics are shown by continuous lines in Figs.3.3(a)-(d) for effective channel lengths of 1.43 μm, 0.63 μm, 0.43 μm, and 0.33 μm respectively .

Table 3.1

The extracted values of the parameters used in the subthreshold slope model given by Eqn.(2.16) for the MOSFETs having effective channel lengths of 0.33 μm, 0.43 μm, 0.63 μm and 1.43 μm.

Channel Length (μm)	γ ($V^{1/2}$)	Γ	s ($V^{-1/2}$)	S (V^{-1})
1.43	0.550498	-0.027129	0.014307	0.004690
0.63	0.590389	-0.005396	0.029623	0.007481
0.43	0.604011	0.024737	0.045488	0.009397
0.33	0.509722	0.023842	0.067303	0.015221

The experimental values of the ideality factor η are obtained by the following expression

$$\eta = \left(\frac{1}{V_T}\right)\left(\frac{\delta ln(I_D)}{\delta V_{GS}}\right)^{-1}. \tag{3.5}$$

Thus, these values are obtained by a first order approximation of the $\ln(I_D)$ versus V_{GS} characteristics for $V_{DS} = 0.1$ V in the subthreshold region of operation, (i.e., for applied $V_{GS} \leq V_{Ts}$). The subthreshold slope (ideality factor) values obtained from the measurement data[13] for $V_{DS} = 0.1$ V are also shown in Figs.3.3(a)-(d) by the diamond symbols. The simulated results are observed to be overestimating the ideality factor, particularly so for small channel lengths (i.e., for all the channel lengths below 1.43 μm). These results are expected since the dependence of η on V_{SB} was not modeled

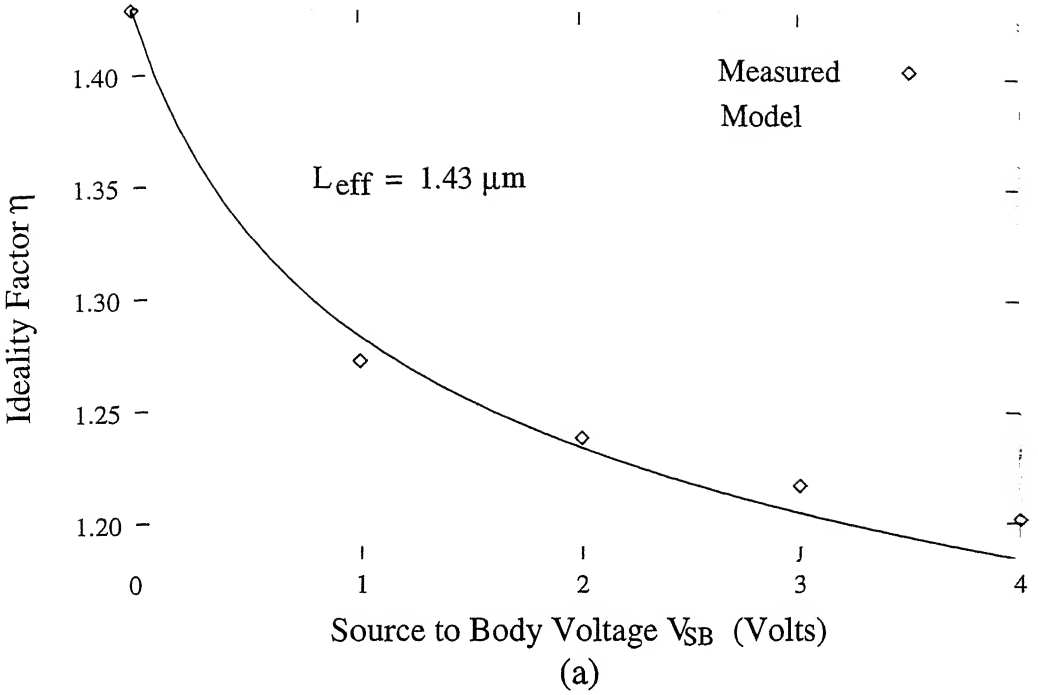
properly by the earlier authors[9].

It has been assumed by Liu et al.[14] that the point x_o along the channel where the surface potential is minimum converges rapidly to $L_{eff}/3$ from the source end for higher values of V_{DS}. Hence, the ideality factor η in its final expression comes out to be independent of the drain voltage V_{DS}[3]. However, this assumption may not quite hold true for small channel length devices, since for these cases, the applied drain voltage modulates the surface potential profile quite markedly, and, hence, the minimum surface potential point may not converge to $L_{eff}/3$, but instead, may become a strong function of V_{DS}. Hence, an improved model for η is needed which explicitly accounts for the effect of V_{DS}. This improved model has been described in detail earlier in the previous chapter, and the results simulated from that model are presented here.

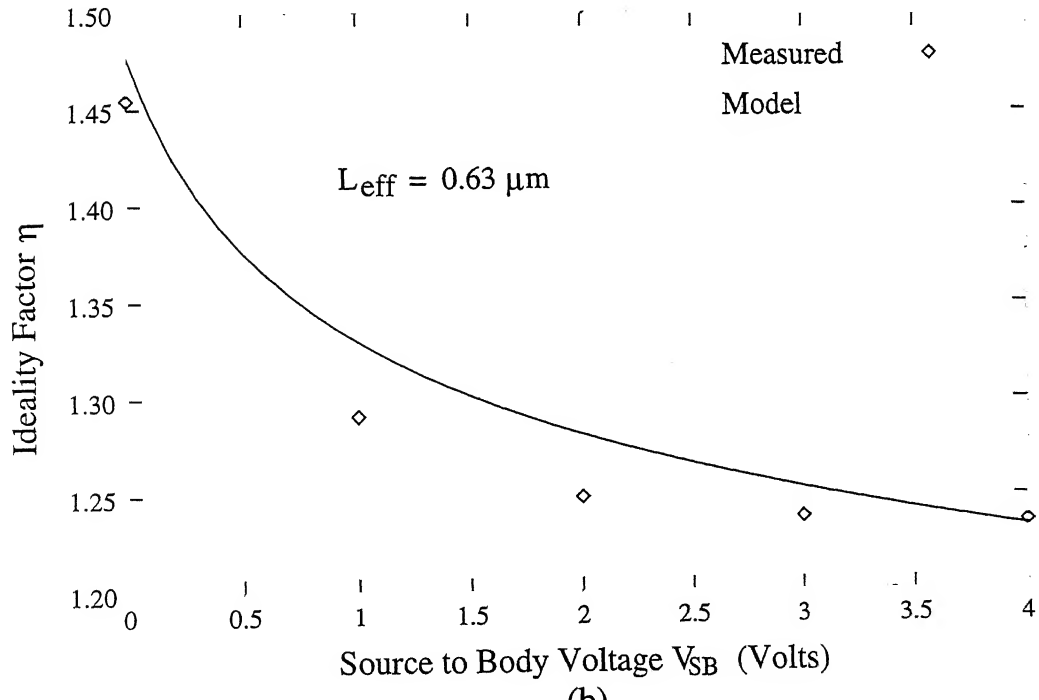
3.1.2 Simulation Results of the Improved Subthreshold Slope Model

In this section, the simulated results of the subthreshold slope model given by Eqn.(2.26) are presented. In the previous chapter, it has been shown that the minimum surface potential point x_o is a function of the applied drain voltage V_{DS}. And since the subthreshold slope (Eqn.(2.26)) is a function of x_o, hence, this model is implicitly V_{DS} dependent.

The surface potential ψ_s along the channel has been calculated with the help of Eqn.(2.19). Then, X_{dep} is calculated using Eqn.(2.18) taking $V_{SB} = 0$ V. The



(a)



(b)

Figure 3.3 (contd.)

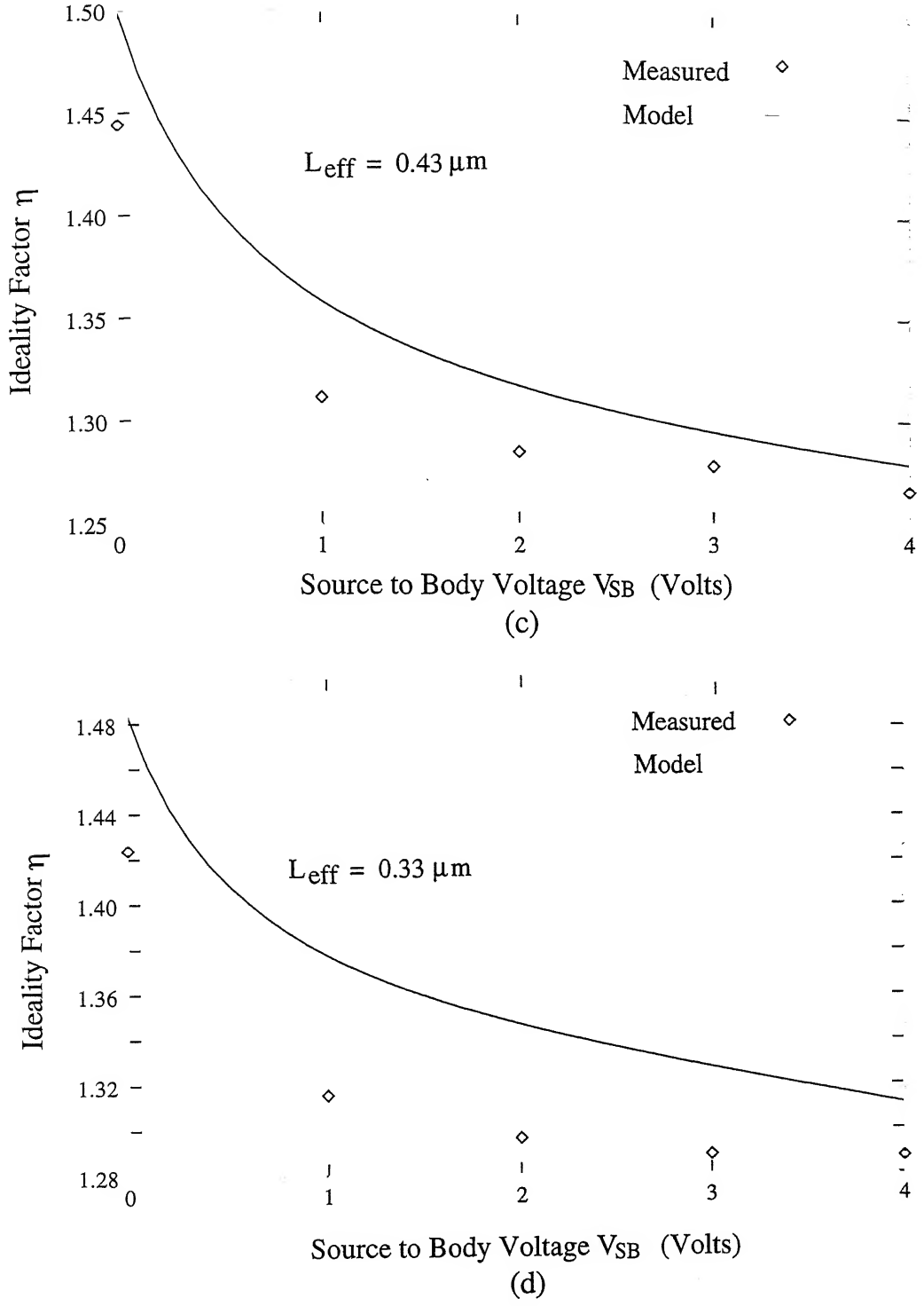


Figure 3.3: Results of the subthreshold slope model [Eqn.(2.16)] at $V_{DS} = 0.1$ V for (a) $L_{eff} = 1.43$ μm, (b) $L_{eff} = 0.63$ μm, (c) $L_{eff} = 0.43$ μm, and (d) $L_{eff} = 0.33$ μm.

characteristic length l is found from this value of X_{dep} using Eqn.(2.22). For this simulation, the value for the fudge factor η_f has been taken to be equal to 1.0, which may not be exactly true. The value of the long channel threshold voltage V_{th0} is calculated from Eqn.(2.21). The calculated values of the channel surface potential ψ_s are plotted with respect to the position along the channel in Fig.3.4 for different channel length devices (i.e., for $L_{eff} = 0.33$ μm, 0.43 μm, and 1.43 μm). The intention of this activity is to check whether the x_o point really lies at $L_{eff}/3$ location irrespective of V_{DS} and L_{eff}. From this figure, it can be clearly seen that for relatively longer channel MOSFETs (e.g., for $L_{eff} = 1.43$ μm), the surface potential is almost uniform along the channel. This implies that the value of x_o is close to $L_{eff}/2$ instead of $L_{eff}/3$ which was assumed in the derivation of the subthreshold slope [Eqn.(2.16)] by Kang et al.[9].

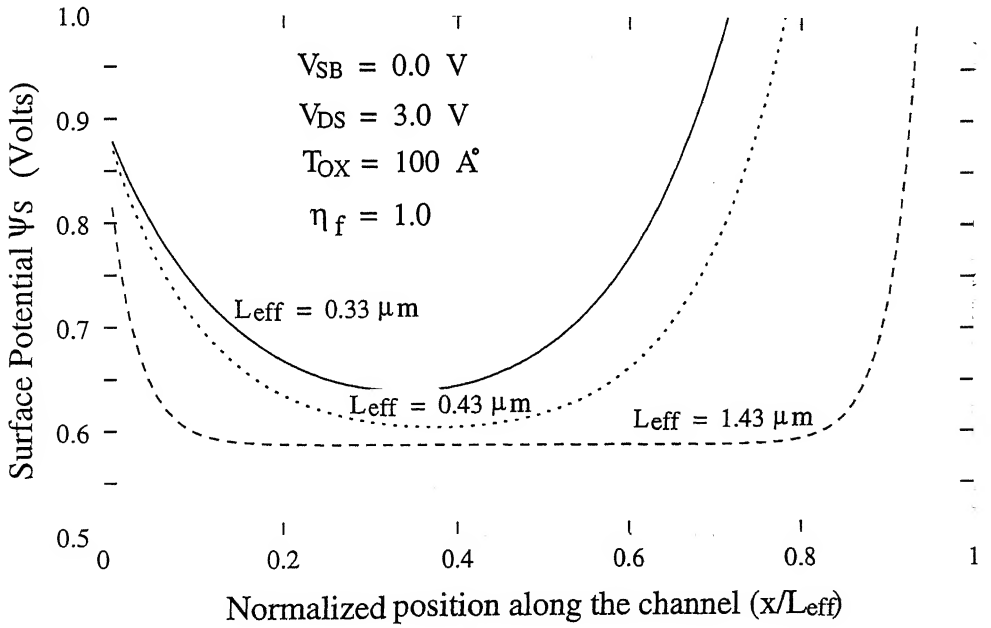
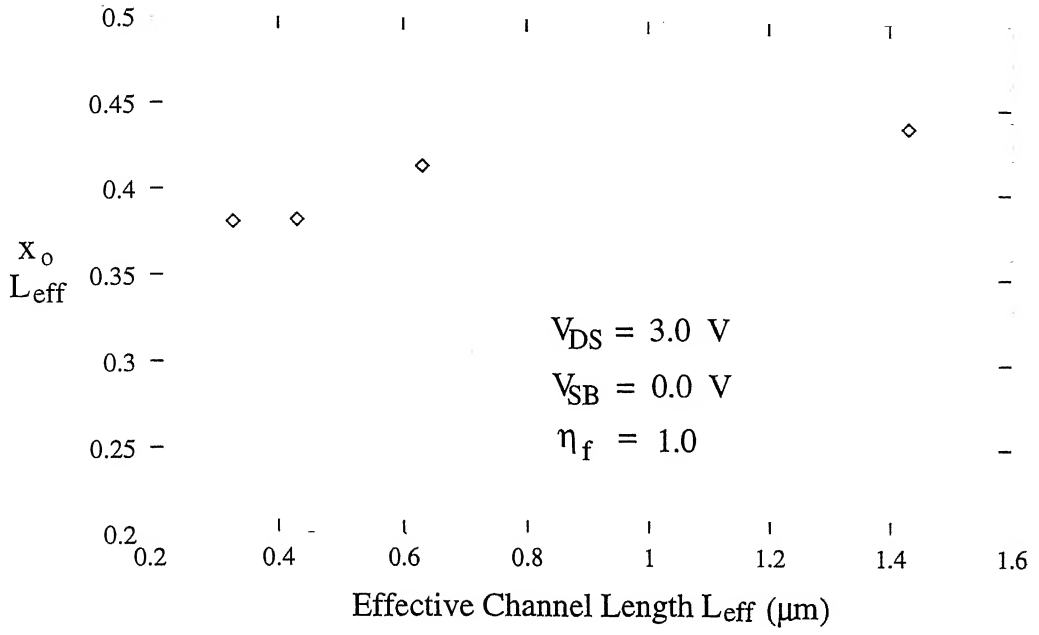


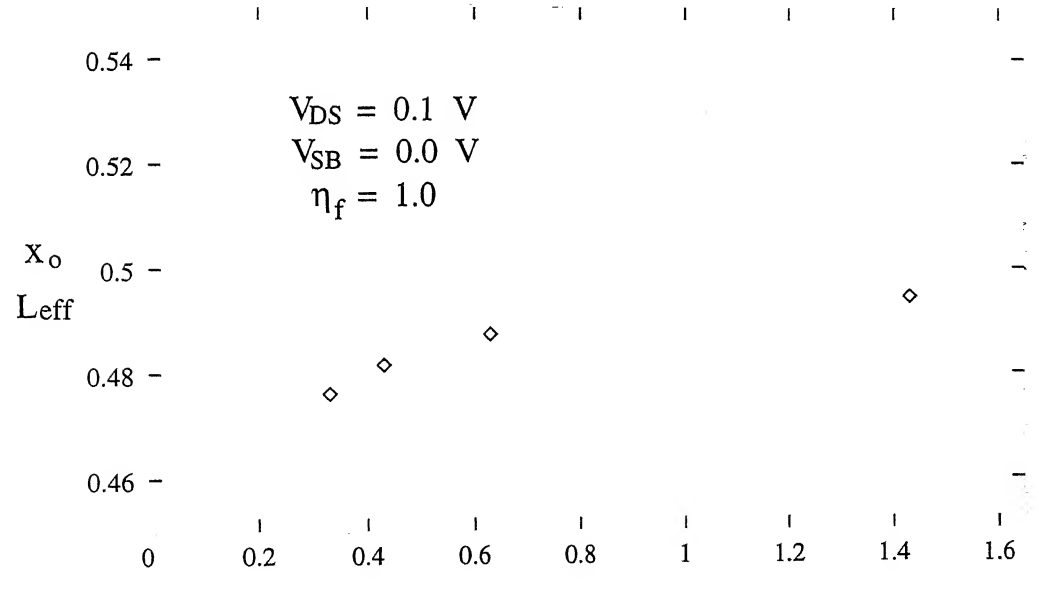
Figure 3.4: The variation of the surface potential $\psi_s(x)$ along the channel for various channel lengths at $V_{DS} = 3.0$ V.

The values of x_0/L_{eff} are found for $V_{SB} = 0$ V from the closed form expression given by Eqn.(2.24), and these are plotted as a function of the effective channel length L_{eff} in Figs.3.5(a) and (b) for $V_{DS} = 0.1$ V and 3.0 V respectively. From these figures, it can clearly be seen that x_o does not converges to $L_{eff}/3$, particularly so for $V_{DS} =$ 0 V, which is expected. Also, for higher values of V_{DS} (e.g., for $V_{DS} = 3$ V), the values of x_o/L_{eff} are much greater than 0.33 (the assumed value in [9,15]) for channel lengths of 0.63 μm and 1.43 μm. In any case, these values are always higher than 0.33, which confirm our earlier prediction of this kind of behavior.

As explained in the previous chapter, the fudge factor η_f appearing in the expression of the characteristics length l [Eqn.(2.22)] is a function of both L_{eff} and V_{SB}. From a comparison between the results obtained from the subthreshold slope model [Eqn.(2.26)] and the measured values of the subthreshold slope from the experimental data, the values of the fudge factor η_f have been found for each channel length and V_{SB}. It has been observed that this fudge factor is a monotonically decreasing function of the channel length. It also decreases drastically as V_{SB} is increased. Therefore, it has been modeled in this work as an exponentially decreasing function of V_{SB}. The expression for this model for the fudge factor η_f is given in Eqn.(2.23). The value of the parameter η_{fo} appearing in the expression for η_f is a strong function of the effective channel length L_{eff} and takes different values for different channel lengths, which are to be extracted from the subthreshold slope data. The coefficient k' is almost constant with an approximate value of 0.75 for all channel lengths. The extracted values of the parameters η_{fo} and k' for different channel length devices are given in Table 3.2.



(a)



(b)

Figure 3.5: Plot of x_o/L_{eff} versus L_{eff} for $V_{SB} = 0.0$ V for (a) $V_{DS} = 3.0$ V and (b) $V_{DS} = 0.1$ V.

The fudge factor η_f has been plotted as a function of V_{SB} in Figs.3.6(a) and (b) for the MOSFETs having effective channel lengths of 0.33 μm and 0.43 μm respectively. In these figures, the fudge factor values calculated from its model [Eqn.(2.23)] are shown by continuous lines, whereas the values obtained from the measured values of the subthreshold slope from the experimental data are shown by the diamonds. An excellent match between the two is seen from the figures.

Table 3.2

The extracted values of the parameters used in the model of the fudge factor η_f [Eqn.(2.23)] for the MOSFETs having effective channel lengths of 0.33 μm, 0.43 μm, 0.63 μm and 1.43 μm.

Channel Length (μm)	η_{fo}	k' $(V)^{-1}$
1.43	1.09	0.75
0.63	1.15	0.735
0.43	1.54	0.73
0.33	2.92	0.75

This model for the fudge factor is used for calculating the value of the minimum surface potential point x_o. The simulated results for the improved subthreshold slope model developed in this work[Eqn.(2.26)] are plotted as a function of V_{SB} in Figs.3.7(a) and (b) for L_{eff} = 0.63 μm and 0.33 μm respectively for V_{DS} = 0.1 V. Figures 3.8(a) and (b) show the same plots for V_{DS} = 3 V. The experimentally measured data are

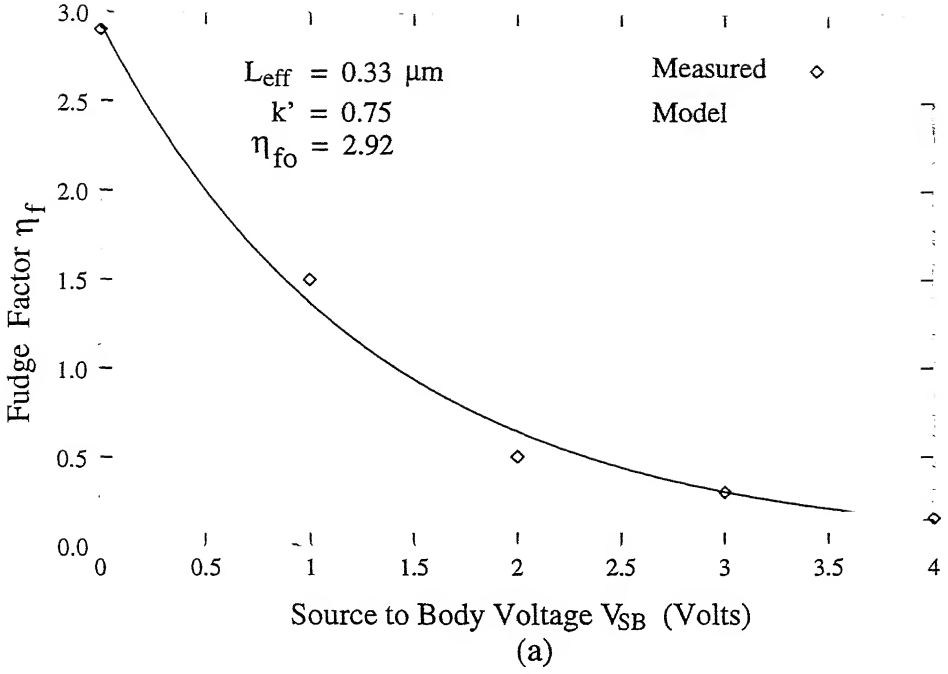
also shown in the figures for the sake of comparison. From these figures, it can clearly be seen that the improved model gives a much better fit to the measured data than the original model, which can be found by comparing these figures with Figs.3.3(c) and (d). Thus, our earlier assertion that the x_o point and thus the ideality factor η are functions of applied V_{DS} and V_{SB} is substantiated.

3.2 The Subthreshold Current Characteristics

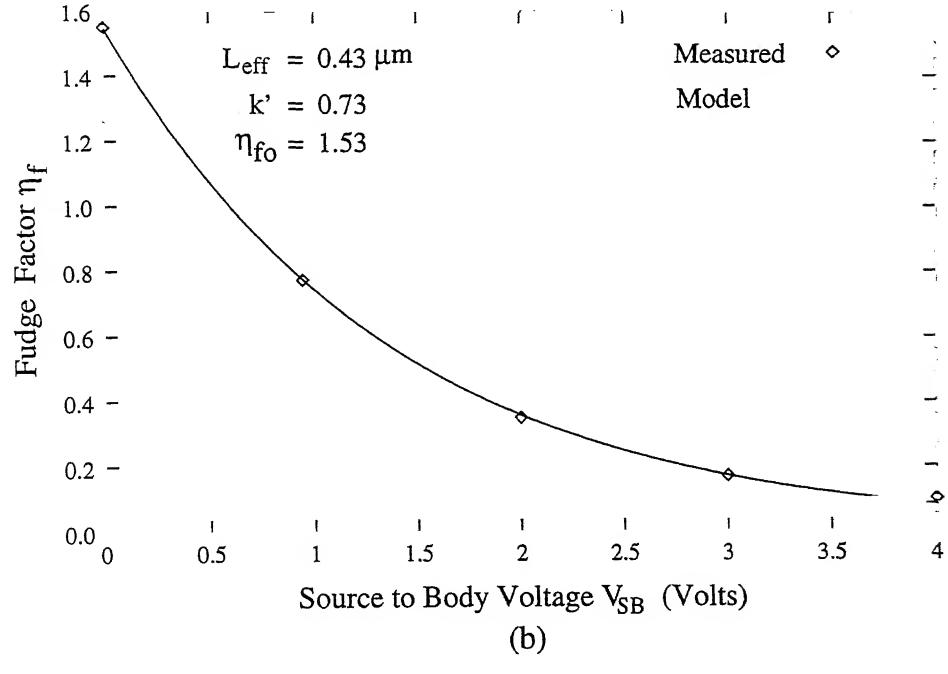
In order to test the performance of the improved subthreshold slope model developed in this work, the I_D-V_{GS} characteristics are simulated for short channel MOSFETs in the subthreshold region. As described in the previous chapter, the subthreshold drain current model developed in this work[Eqn.(2.27)] uses the modified and improved subthreshold slope model based on the threshold voltage data given by the BSIM threshold voltage model[Eqn.(2.3)].

The performance of the subthreshold drain current model developed in this work is tested with the experimental data on short channel MOSFETs reported in literature [16,17]. The I_D-V_{GS} characteristics of a MOSFET having an effective channel length of 0.075 μm and an oxide thickness of 70$\AA$ have been given by Rittenhouse et al.[17] for $V_{SB} = 0$ V and for V_{DS} values ranging from 0.05 V to 2.5 V in steps of 0.245 V.

In order to determine the values for the subthreshold slope η, one needs to extract the values of the parameters γ, Γ, s, and S from the data of threshold voltage



(a)



(b)

Figure 3.6: The simulated plots for the fudge factor η_f versus V_{SB} for (a) $L_{eff} = 0.33$ μm and (b) $L_{eff} = 0.43$ μm.

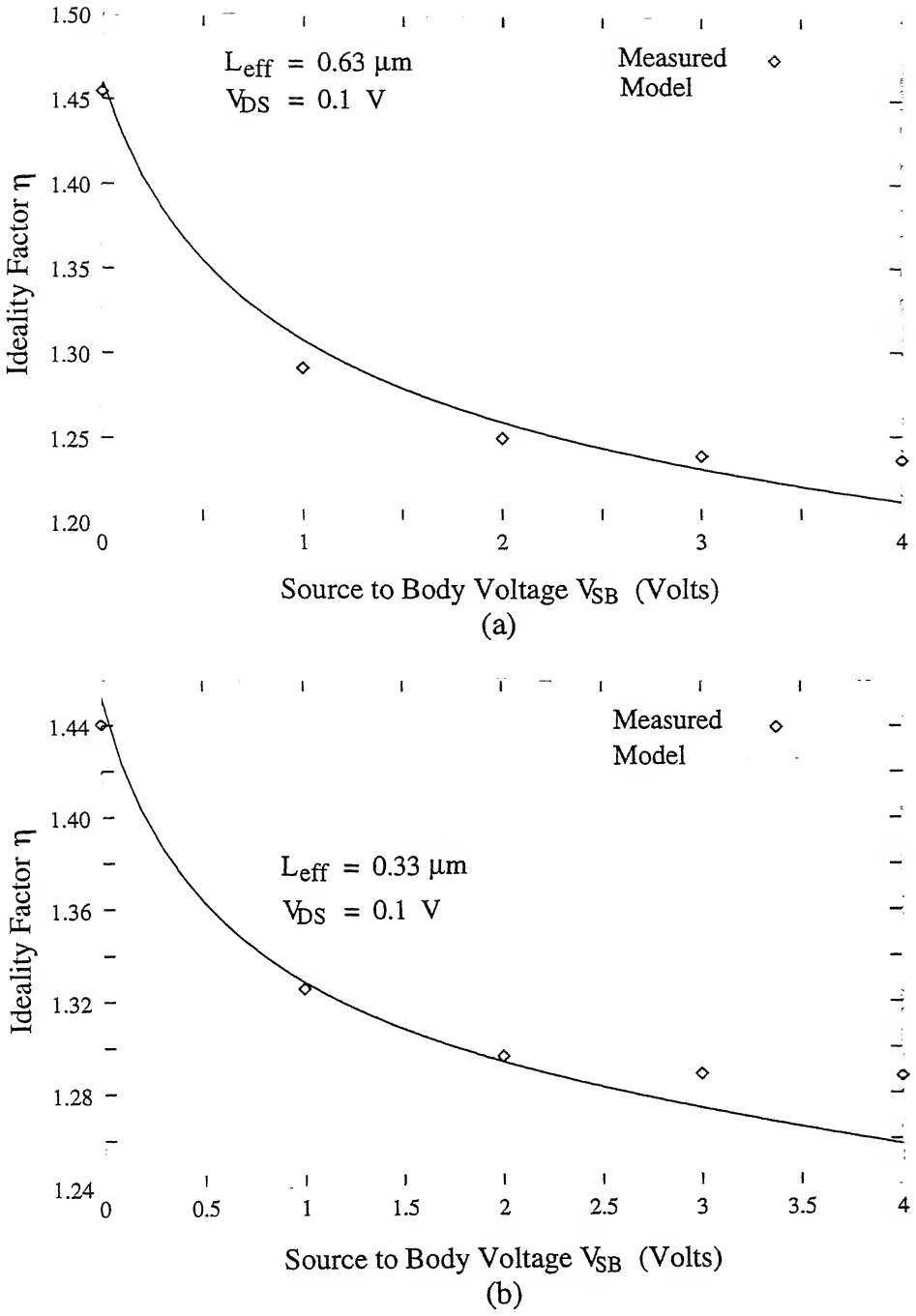


Figure 3.7: The simulated plots of the ideality factor η obtained from the improved subthreshold slope model [Eqn.(2.26)] for $V_{DS} = 0.1$ V for (a) $L_{eff} = 0.63$ μm and (b) $L_{eff} = 0.33$ μm.

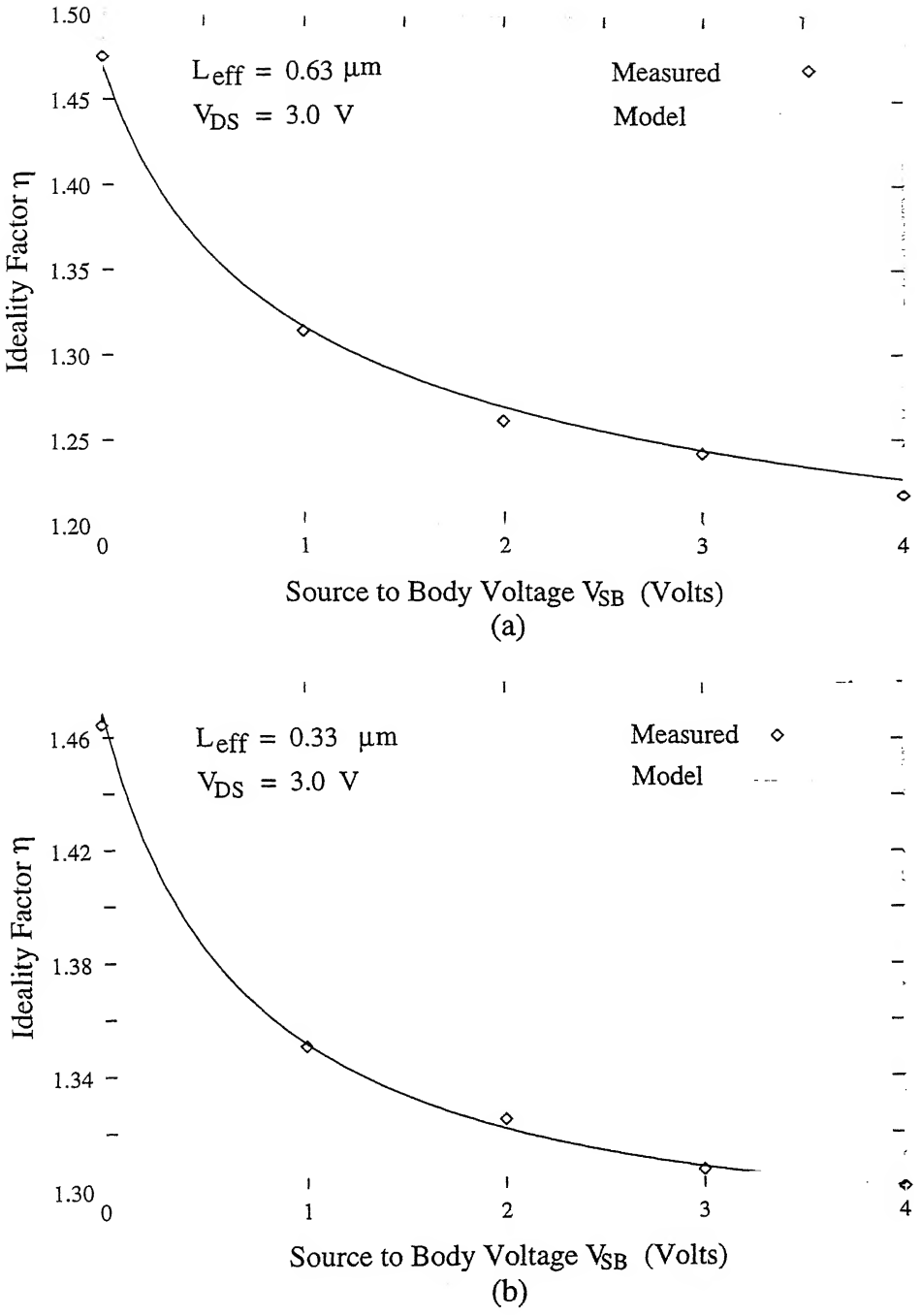


Figure 3.8: The simulated plots of the ideality factor η obtained from the improved subthreshold slope model [Eqn.(2.26)] for $V_{DS} = 3.0$ V for (a) $L_{eff} = 0.63$ μm and (b) $L_{eff} = 0.33$ μm.

variation with respect to the substrate potential V_{SB}. This requires the I_D-V_{GS} characteristics for different values of V_{SB}. Unfortunately, these data are not presented by Rittenhouse et al.[17]. However, from Eqn.(2.26), it can be seen that the value of the parameter η can be extracted from the value of the parameter σ, and in reality, the exact values of the parameters s and S are not needed. The values for the parameter σ can be extracted from the threshold voltage versus V_{DS} curve, which are found to be 0.435 for these cases. Similarly, the values of the parameters γ and Γ can be extracted by simulating Eqn.(2.26) for one value of the measured subthreshold slope. For finding the value of x_o/L, Eqn.(2.24) is used in which the value of the parameter k' has been extracted earlier. The subthreshold slope model results are plotted in Fig.3.9, along with the experimentally measured values for the sake of comparison. An excellent match is seen from the figure, which stakes the claim that the subthreshold slope model developed in this work is very accurate even for the sub-0.1 micron channel length MOSFETs. This model of the subthreshold slope has been used in the drain current model.

The simulated I_D-V_{GS} characteristics in the subthreshold region using the improved subthreshold slope model for this device are shown in Fig.3.10, where the experimentally obtained results[17] are also shown for the sake of comparison. From Fig.3.10, it is seen that the simulated results obtained from the subthreshold drain current model developed in this work show a good match with the experimental data, particularly in the deep subthreshold region. In the moderate inversion region, the performance of our model deteriorates. This is a problem of the global parameter extraction approach

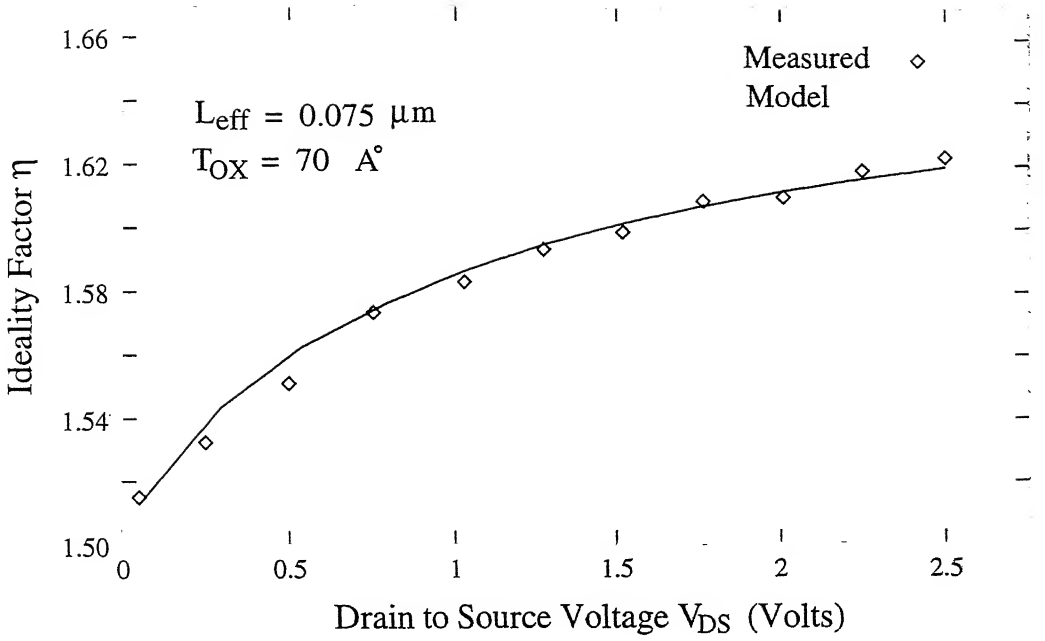


Figure 3.9: Comparison of the subthreshold slope calculated from our improved subthreshold slope model [Eqn.(2.26)] with the subthreshold slope obtained from the experimentally measured data reported by Rittenhouse et al.[17] for a 0.075 μm channel length device.

as has been elaborated by Deshpande and Dutta[10].

The simulated results of our subthreshold slope model and the I_D-V_{GS} characteristics have been compared with the experimental data reported on another sub-0.1 micron MOSFET, where the effective channel length was 0.09 μm, and the oxide thickness was 35 $\AA$ [16]. The I_D-V_{GS} characteristics have been given for $V_{DS} = 0.05$ V and 1.55 V by Mii et al.[16]. The values of the model parameters γ, Γ, s, and S are extracted by the method similar to the one applied for the 0.075 μm channel length device. The subthreshold slope model results are plotted in Fig.3.11 along with the experimentally

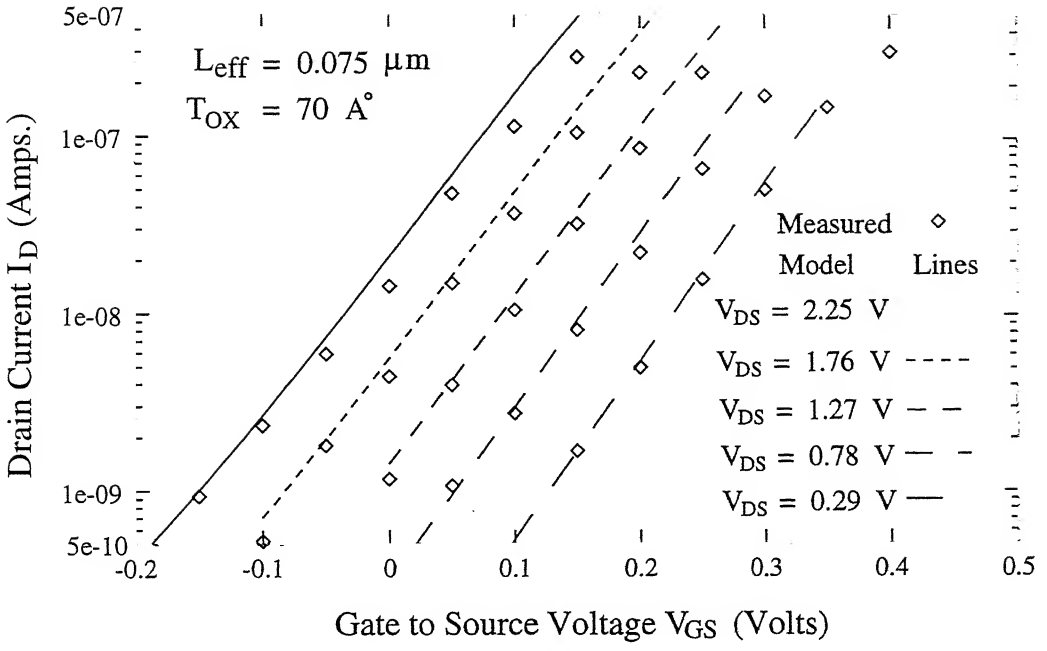


Figure 3.10: Comparison of the I_D-V_{GS} characteristics calculated from our model with the experimental data reported by Rittenhouse et al.[17] for a 0.075 μm channel length device.

obtained values[16] for the sake of comparison. It is observed that the match between the two is quite good.

The simulated I_D-V_{GS} characteristics in the subthreshold region for the 0.09 μm channel length MOSFET reported by Mii et al.[16] are shown in Fig.3.12, where the experimentally obtained results are also shown for comparison. This figure shows a good match between the simulated results and the experimentally obtained results.

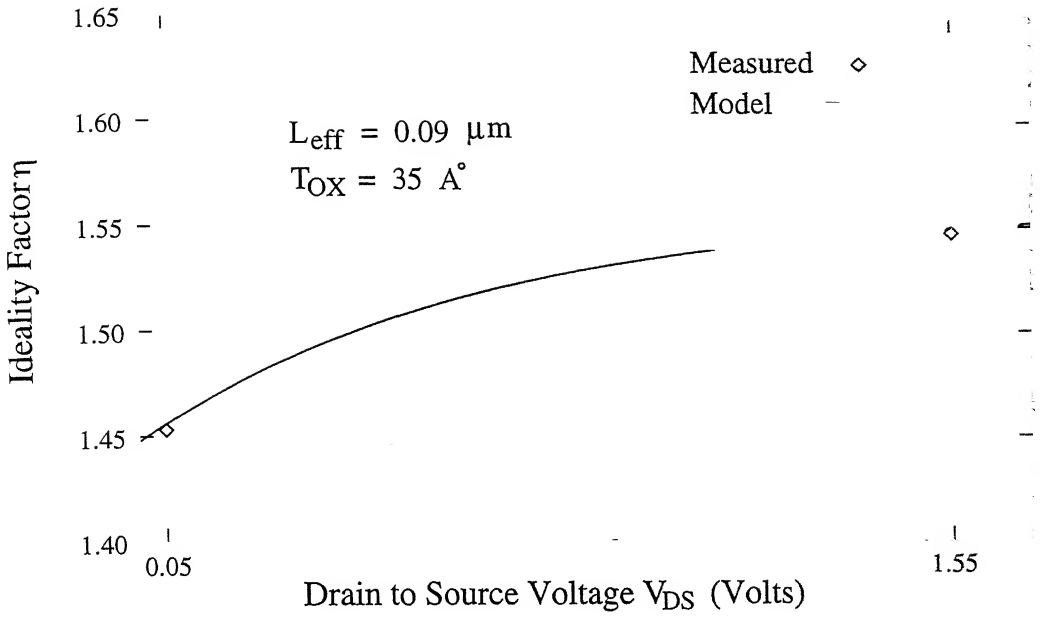


Figure 3.11: Comparison of the subthreshold slope calculated from our improved subthreshold slope model [Eqn.(2.26)] with the subthreshold slope obtained from the experimental data reported by Mii et al.[16] for a 0.09 μm channel length device.

3.3 Results of the Complete Drain Current Model

The complete model for the drain current, valid for all regions of operation, has been described in the previous chapter. The threshold voltage model and the subthreshold slope model developed in this work are used in the complete model given by Deshpande and Dutta[10]. The complete model, described in detail in Section 2.8, has been simulated for the 0.075 μm and 0.09 μm channel length MOSFETs reported by Rittenhouse et al.[17] and Mii et al.[16] respectively. The complete I_D-V_{GS} characteristics simulated from the model are plotted for the 0.075 μm channel length MOSFET in Fig.3.13 along

with the experimentally obtained values[17]. Similarly, same characteristics are plotted in Fig.3.14 for the 0.09 μm channel length MOSFET reported by Mii et al.[16]. The results show a very good match.

The simulated I_D-V_{DS} characteristics are plotted in Fig.3.15 for different values of the applied gate voltage V_{GS} for the 0.075 μm channel length MOSFET, along with the experimentally obtained results reported by Rittenhouse et al.[17].

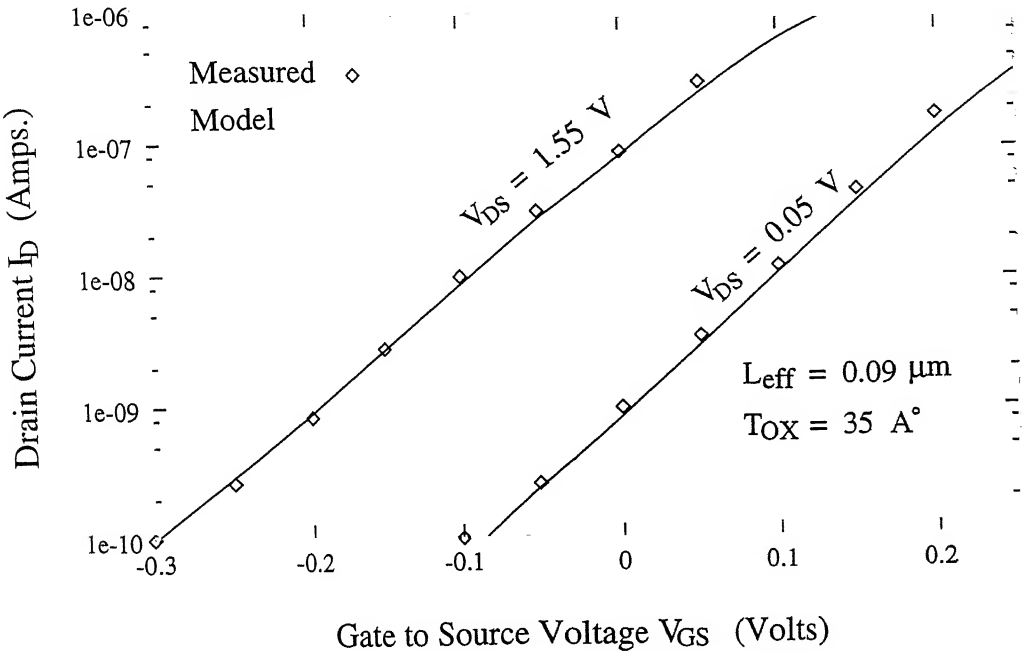


Figure 3.12: Comparison of the I_D-V_{GS} characteristics in the subthreshold region calculated from our model with the experimental data reported by Mii et al.[16] for a 0.09 μm channel length device.

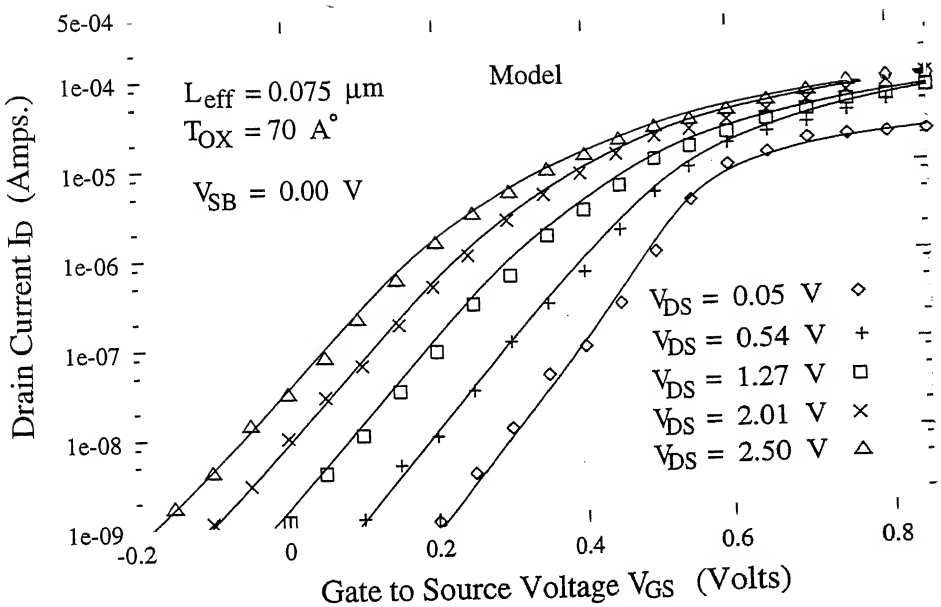


Figure 3.13: Comparison of the I_D-V_{GS} characteristics calculated from our model with the experimental data reported by Rittenhouse et al.[17] for a 0.075 μm channel length device.

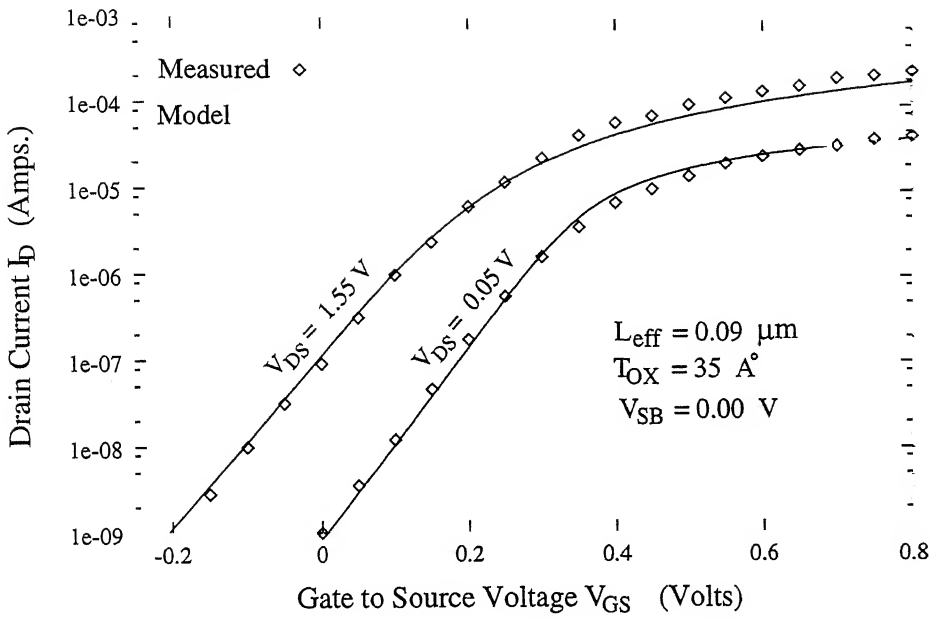


Figure 3.14: Comparison of the I_D-V_{GS} characteristics calculated from our model with the experimental data reported by Mii et al.[16] for a 0.09 μm channel length device.

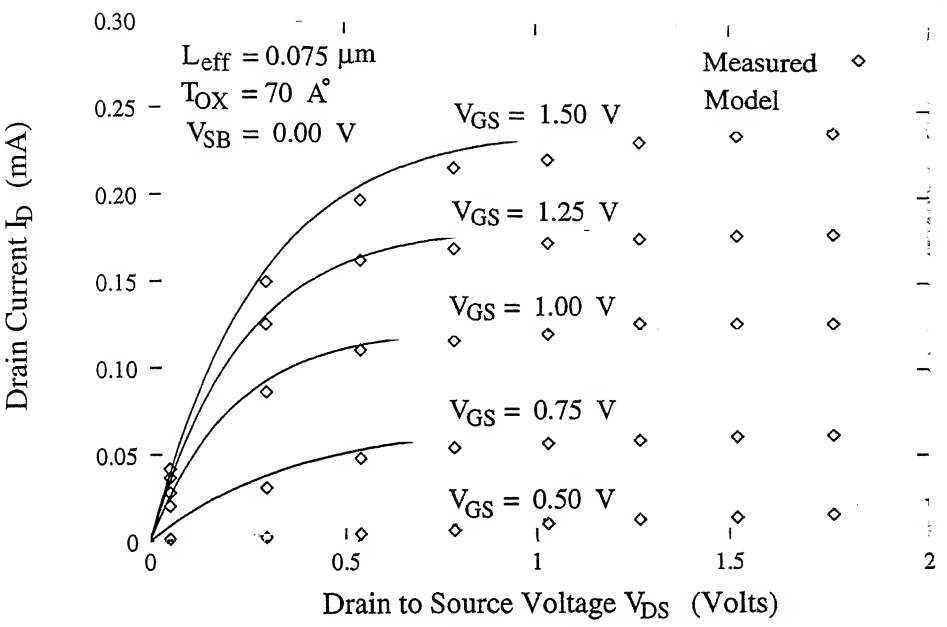


Figure 3.15: Comparison of the I_D-V_{DS} characteristics calculated from our model with the experimental data reported by Rittenhouse et al.[17] for a 0.075 μm channel length device.

Chapter 4

Summary and Conclusion

The emergence of the analog integrated circuits and mixed-signal VLSI chips demands very accurate and elaborate MOSFET models suitable for circuit simulation. The MOSFET models which satisfy the requirements of digital circuit simulation are currently no longer useful for analog circuit simulation. Therefore, MOSFET modeling suitable for analog circuit simulation has become one of the most challenging fields in the VLSI area. Also, very high packing density achieved by the reduction of the size of an individual transistor in the IC chip has become possible by the improvements in the photolithography techniques. This high packing density created high power dissipation problem. Thus, low operating current and voltage designs are becoming popular because of their inherent advantages in reducing the power dissipation, which needs to be kept within limit. The low voltage operation pushes the MOSFET into its weak inversion region. In addition to this, quite a few battery operated applications use the MOSFETs in their subthreshold region. Hence, it has become imperative to accurately

model the MOSFET in its subthreshold region.

4.1 Summary of the Work

The work done is summarized in this section. Initially, the subthreshold slope model proposed by Kang et al.[9] has been simulated in this work. For this simulation, the various parameters used in the model are extracted from the threshold voltage data. The simulation of this subthreshold slope model is done for MOSFETs having effective channel lengths of 0.33 μm, 0.43 μm, 0.63 μm, and 1.43 μm. These simulated results have been compared with the experimentally obtained results of the subthreshold slope from the data reported by Lee and Min[13] for these device. It has been observed from this simulation that the simulated results of the subthreshold slope overestimate its measured values, more so for the MOSFETs having relatively shorter channel lengths (e.g., for $L_{eff} = 0.43$ μm, 0.63 μm, and 0.33 μm). This is due to the improper modeling of the drain voltage dependence of the subthreshold slope by Kang et al.[9].

This subthreshold slope model is based on the capacitor equivalent circuit of the MOSFET in the subthreshold region. The subthreshold slope equation of this model is analytically expressed in terms of the parameters of the BSIM threshold voltage model[6] by carefully interpreting it with the capacitor equivalent circuit of the MOSFET in the subthreshold region. In this model, it has been assumed that the distance of a point on the channel from the source where the surface potential is minimum converges rapidly to a value equal to $L_{eff}/3$ as the drain voltage is increased.

Thus, the drain voltage dependence of this minimum surface potential point has been neglected by Kang et al.[9]. Hence, the subthreshold slope expression obtained in their work comes out to be independent of the drain voltage. However, experimental data on the short channel devices reported in the literature show that the subthreshold slope is a strong function of the drain voltage. Thus, this model has a major flaw, which makes it highly unsuitable for the simulation of short channel MOSFETs in their subthreshold region of operation. In this work, this model has been modified in order to develop a more accurate subthreshold slope model which takes into account the effects of the drain voltage, as well as that of the effective channel length, and the body voltage on the subthreshold slope.

In order to develop this improved model, the distance of the minimum surface potential point x_o is evaluated for various values of L_{eff} and V_{DS} from the analytical expression given by Liu et al.[14], after making some modifications, as detailed earlier in Chapter 2. This model of x_o has been used in the original subthreshold slope model developed by Kang et al.[9]. Thus, a new and improved subthreshold slope model is obtained in this work. The values of the parameters γ, Γ, s, and S used in the improved subthreshold slope model have to be extracted from the threshold voltage data. These parameters are used to model the various short channel effects. In addition to these four parameters, this model has one more fitting parameter η_f, whose value is to be extracted from the measurement data for short channel MOSFETs. The simulation of this improved subthreshold slope model is done for MOSFETs having effective channel lengths ranging from 0.075 μm to 1.43 μm, and the simulated results are observed to

be matching quite closely with the measured values of the subthreshold slope. This improved subthreshold slope model is based on a true physical foundation of device physics. It has been made accountable for the DIBL effect along with the dependence of the subthreshold slope on the various parameters such as the effective channel length, the body voltage, and the drain voltage.

The drain current model of Deshpande and Dutta[10] is modified in this work by replacing the subthreshold slope model and the threshold voltage model used in it by the improved subthreshold slope model developed in this work and the BSIM threshold voltage model respectively, in order to arrive at a new drain current model. This new drain current model is simulated for MOSFETs having effective channel lengths of 0.075 μm and 0.09 μm reported by Rittenhouse et al.[17] and Mii et al.[16] respectively. The results obtained from this simulation are observed to be matching very well with the experimentally obtained results.

4.2 Conclusion

1. The subthreshold slope model developed by Kang et al.[9] is derived after assuming that the value of x_o (i.e., the distance of a point on the channel from the source where the surface potential is minimum) is equal to $L_{eff}/3$, independent of the drain voltage and the effective channel length. However, this is not true. The value of x_o is observed to be strongly dependent on the various parameters such as the drain voltage, the body voltage, and the effective channel length.

Therefore, in order to model the effect of the drain voltage on the subthreshold slope, it is important to model x_o in terms of these parameters.

2. In this work, in the calculation for the value of x_o, we have used a fitting parameter, referred to as the fudge factor η_f. This has been done in order to compensate for the invalid assumption of a constant depletion layer thickness along the channel in the subthreshold region. It has been observed that the value of the fudge factor decreases as the effective channel length is increased, and it finally converges to a value equal to unity for MOSFETs having longer channel lengths. Also, the value of the fudge factor decreases exponentially with an increase in the body voltage V_{SB}. Though the fudge factor is modeled as a fitting parameter in this work, however, its behavior with respect to the effective channel length and the body voltage implies that it represents a true physical phenomenon due to the non-uniform depletion layer thickness along the channel of the MOSFET. Thus, this parameter η_f has a well justified physical meaning.

4.3 Future Scope of Improvement

As explained in the previous section, the fudge factor η_f has a physical meaning. However, in this work its value has to be extracted from the measurement data, and the exact dependence of this fudge factor value on the substrate doping, effective channel length and oxide thickness can not be defined at this moment. The subthreshold model developed in this work can be improved by analytically expressing this fudge factor in

terms of the terminal voltages and the device specifications such as the effective channel length, the oxide thickness, and the substrate doping.

References

1. C.A. Laber and P.R. Gray, "A 20 MHz sixth order BiCMOS parasitic-insensitive continuous-time filter and second order equalizer optimized for disk-drive read channels," IEEE J. Solid State Circuits, Vol.28, No.4, pp.462-470, 1993.

2. I.A. Young, J.K. Greason, and K.L. Wong, "A PLL clock generator with 5 to 100 MHz of locking range for microprocessors," IEEE J. Solid State Circuits, Vol.27, No.11, pp.1599-1607, 1992.

3. Y.P. Tsividis and K. Suyama, "MOSFET Modeling for Analog Circuit CAD: Problems and Prospects," IEEE J. Solid-State Circuits, Vol.29, No.3, pp.210-216, 1994.

4. Y.P. Tsividis and G. Masetti,"Problems in Precision Modeling of the MOS Transistor for Analog Applications," IEEE Trans. Computer-Aided Design, Vol.CAD-3, No.1, pp.72-79, 1984.

5. R.R. Troutman,"Subthreshold Design Considerations for Insulated-Gate FET," IEEE J. Solid State Circuits, Vol.SC-9, No.2, pp.55-60, 1974.

6. B.J. Sheu, D.L. Scharfetter, P.K. Ko, and M.C. Jeng,"BSIM: Berkeley Short Channel IGFET Model for MOS Transistors," IEEE J. Solid State Circuits, Vol.SC-22, No.4, pp.558-566, 1987.

7. M. Shur, T.A. Fjeldly, T. Ytterdal, and K. Lee,"Unified MOSFET Model," Solid State Electronics, Vol.35, No.9, pp.1795-1802, 1992.

8. N.D. Arora, R. Rios, C.L. Huang, and K. Raol,"PCIM: A Physically Based Continuous Short-Channel IGFET Model for Circuit Simulation," IEEE Tran. Electron Devices, Vol.41, No.6, pp.988-997, 1994.

9. S.W. Kang, K.S. Min, and K. Lee, " Parametric Expression of Subthreshold Slope Using Threshold Voltage Parameters for MOSFETs Statistical Modeling," IEEE Tran. Electron Devices, Vol.43, No.9, pp.1382-1386, 1996.

10. D.R. Deshpande and A.K. Dutta,"A Unified Model for Submicron MOSFETs," accepted for publication in Microelectronic Journal, 1998.

11. Y.P. Tsividis,Operation and Modeling of the MOS Transistor, McGraw-Hill, 1987.

12. R.V. Booth, M.H. White, H.S Wong, and T.J. Krutsick, "The effect of Channel Inplants on MOS Transistor Characterization," Vol.ED-34, No.12, pp.2501-2508, 1987.

13. K. Lee and K.S. Min, Private Communication.

14. Z.H. Liu, C. Hu, J.H. Huang, T.Y. Chan, M.C. Jeng, P.K. Ko, and Y.C. Cheng, "Threshold Voltage Model for Deep-Submicron MOSFETs," IEEE Tran. Electron Devices, Vol.40, No.4, pp.86-95, 1993.

15. T.W. Tang, Q.L. Zhang, and D.H. Navon,"Analytical Model for Threshold Voltage in Submicrometer Channel MOSFETs," IEEE Tran. Electron Devices, Vol.ED-32, pp.1890-1893, 1985.

16. Y. Mii, S. Riston, Y. Taur, D. Kern, T. Lee, K.A. Jenkins, D. Quinlan, T. Brown Jr., D. Danner, F. Sewell, and M. Polcari, "Experimental High Performance sub-0.1 μm Channel nMOSFETs," IEEE Electron Device Lett., Vol.15, No.1, pp.28-30, 1994.

17. G.E. Rittenhouse, W.M. Mansfield, A. Kornblit, R.A. Cirelli, D. Tomes, and G.K. Celler, "Sub-0.1 μm NMOS Transistors Fabricated Using Laser-Plasma Point-Source X-Ray Lithography," IEEE Electron Device Lett., Vol.16, No.7, pp.322-324, 1995.